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Issue 7/2006

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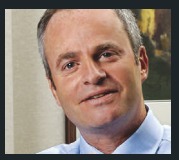

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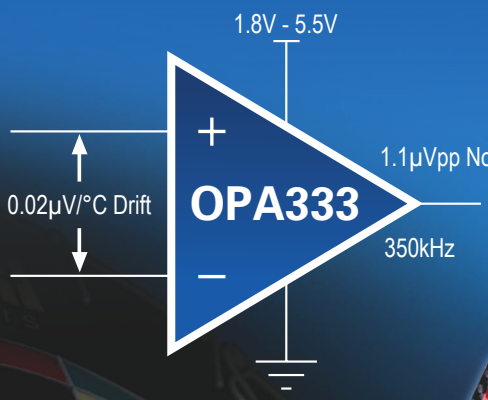

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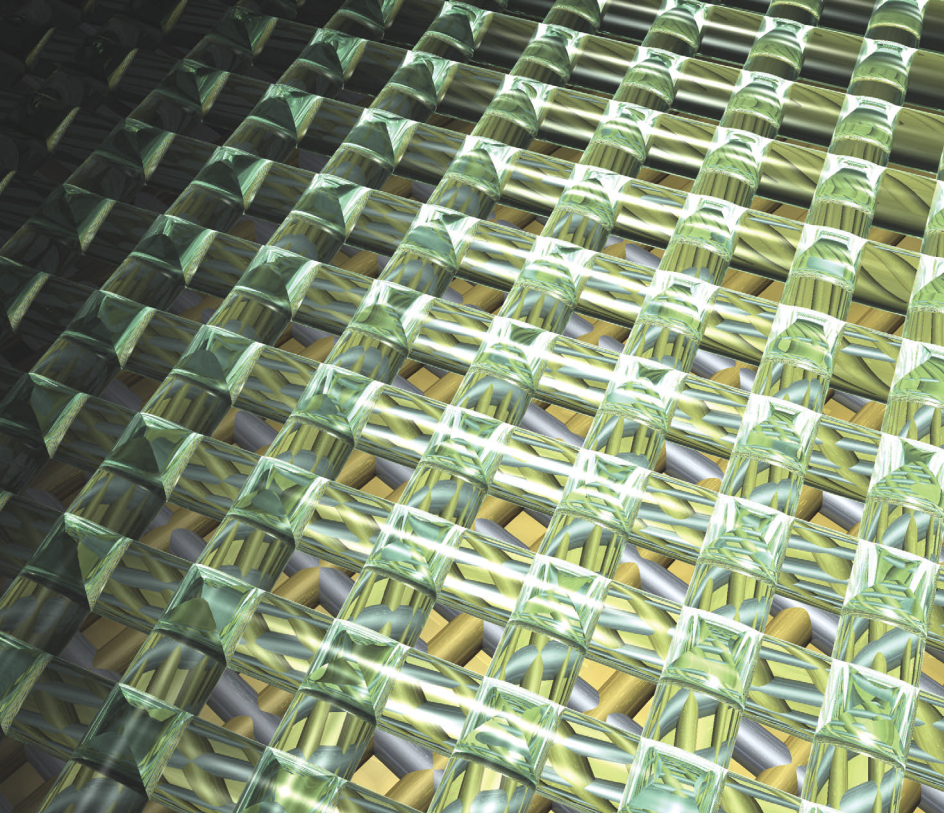

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50 years

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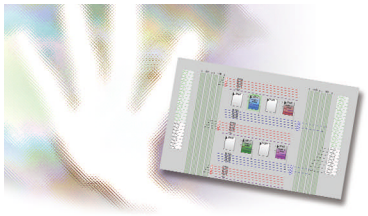

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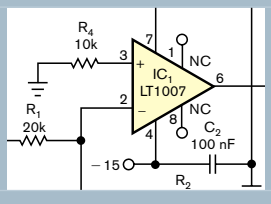

95 On/off buffer switches analog or digital signals

96 Single switch serves dual duty in small, microprocessor-based system

98 Isolated-FET pulse driver reduces size, power consumption

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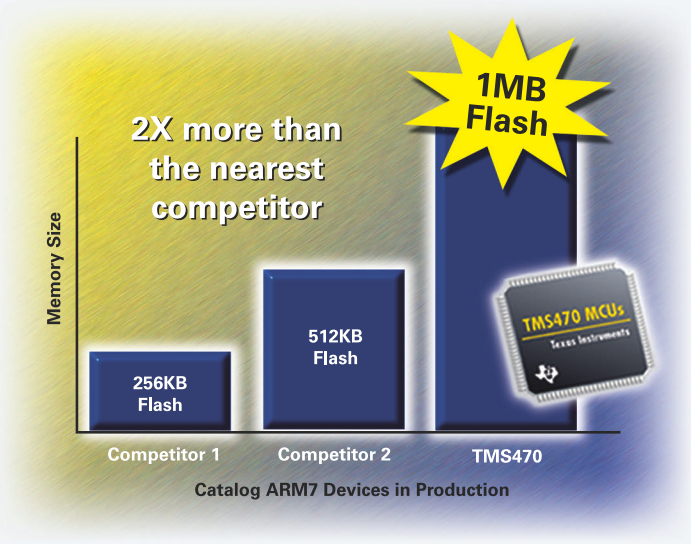

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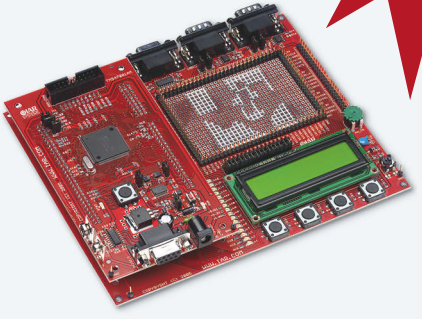

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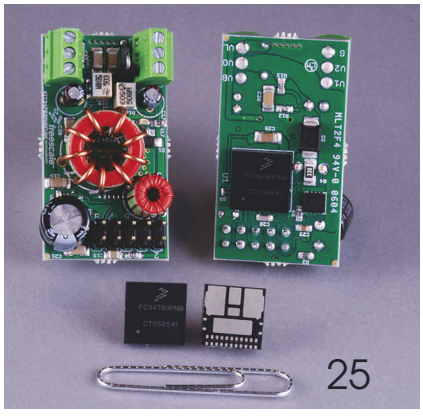

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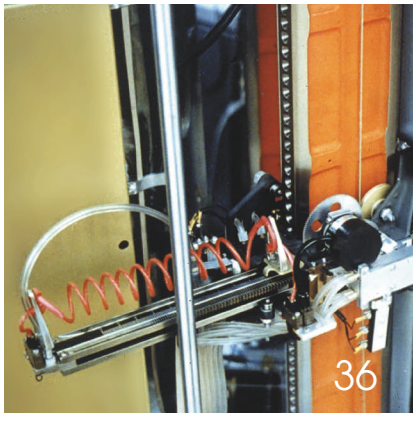

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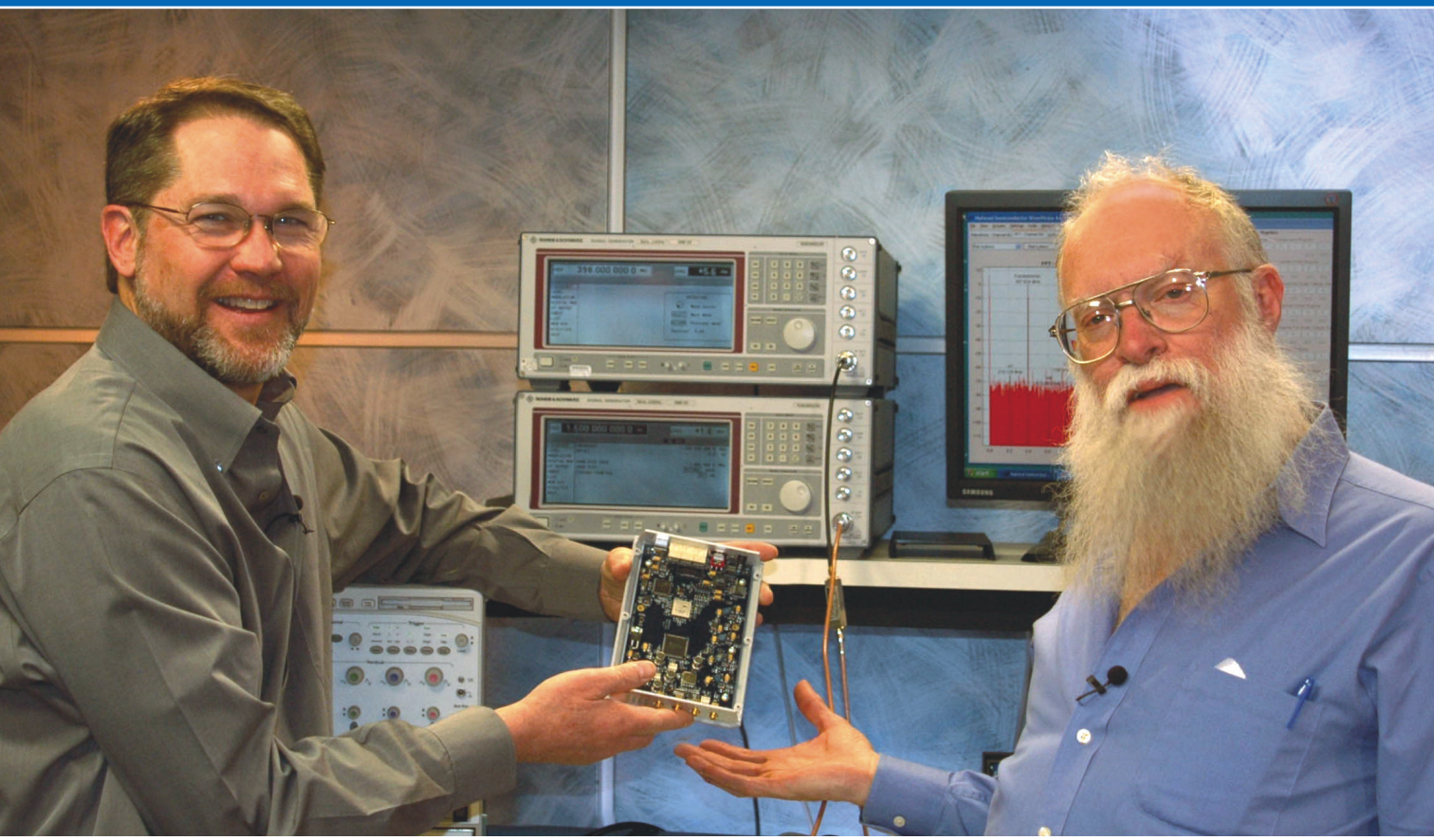
Watch Bob Pease and Dr. Howard Johnson Get Real About High-Speed Data Transfer



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If you have to generate an analog voltage proportional to the module of a vector whose components are also available in analog form, you can adopt a classic solution involving the use of analog multipliers.
→ www.edn.com/article/CA6312102

DFM tool helps with "lithography-friendly" layouts

Mentor Graphics claims that its latest DFM (design-for-manufacturing) offering will help IC designers make "lithography-friendly" IC layouts.
→ www.edn.com/article/CA6313706

Microcontroller vendors further encroach on SOCs

Vendors of high-end microcontrollers are smelling opportunity that in the past might have gone automatically to OEM-designed SOCs (systems on chips).
→ www.edn.com/article/CA6312649

Connectivity activity: Wireless USB, Bluetooth, DLNA

When it comes to digital-consumer gadgets, the term "stand alone" simply does not compute. It's all about connectivity.
→ www.edn.com/article/CA6316098

Serial links take on roles in clamshell-design connections

Designers struggle with reliable ways to connect a screen to the main electronics subsystem, especially in phones and cameras in which the upper half of the shell can rotate.
→ www.edn.com/article/CA6312719

READER'S CHOICE

A selection of recent articles receiving high traffic on www.edn.com.

Design Idea: Simple digital filter cleans up noisy data

Clean up data from pressure and temperature sensors.
→ www.edn.com/article/CA6309111

Design Idea: Low-cost audio filter suppresses noise and hum

Passive filter requires no dc power.
→ www.edn.com/article/CA6309113

Stanley's Law: IC design follows pc-board design

An old friend made a brilliant observation: "Everything that happens in IC design, happened in pc-board design many years ago."
→ www.edn.com/article/CA6309115

Antenna tunes in to needs of satellite-radio designers

Sarantel's antenna has won a spot in the soon-to-ship generation of portable satellite-radio receivers built for the XM Satellite Radio service.
→ www.edn.com/article/CA6311792

Linux joins the consumer-electronics revolution

Designers are turning to the Linux operating system to meet the escalating user-interface, networking, and multimedia requirements of today's consumer-electronics products.
→ www.edn.com/article/CA6305349

FROM THE VAULT

Articles and extras from the EDN *archives that relate to this issue's contents.*

TERMINATOR II (pg 38):

Terminator

Part one of Howard Johnson's series appeared in the March 3 issue.
→ www.edn.com/article/CA6309116

SCALING: A BALANCED VIEW (pg 40):

Ripples in the process pool
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EPIC UPDATES STRETCH STACKABLE SYSTEMS (pg 52):

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EPIC computer pushes temperature extremes
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PC/104 Consortium to take over EPIC
→ www.edn.com/article/CA498707

DESIGNING MICROCONTROLLERS WITH LOW-COST RECONFIGURABILITY (pg 43):

One design fits all
→ www.edn.com/article/CA6255076

BY MAURY WRIGHT, EDITOR IN CHIEF

Happy birthday to us

It's a special birthday for *EDN* this year: our 50th. Some of you may have noticed the 50th-anniversary logo that we've included in *EDN* in recent issues. We've also begun running excerpts in the Pulse section from issues that span our past. We have quite a bit more in store for you as the year goes on. This issue, we launch "Milestones That Mattered," a page that will run monthly through the end of the year. We will choose milestones from our 50-year history that were important when they first occurred and that, even after five decades, still have an effect on key technologies.

Our first milestone is the IBM 305 RAMAC computer (pg 36) that IBM launched in September 1956, just a few months after the May launch of *EDN* as a stand-alone publication. *EDN* then covered all types of electronic end products and enabling technologies with which engineers could build products. A computer filled the bill in those days even though it was decidedly targeted at what we'd now call "information technology." But RAMAC, with its 350 Disk File, also laid the foundation for the disk drives of today that enable everything from MP3 players to personal video recorders to industrial-control systems—and computers.

The IBM RAMAC (random-access-method-of-accounting-and-control) computer was the first digital computer to use a disk drive and that allowed near-real-time manipulation of database records (courtesy Magnetic disk Heritage Center).

The occasion of our golden anniversary also led us to look back at other special issues of *EDN*. In the 1970s, *EDN* was the first publication to provide in-depth coverage of microprocessors. In the 1980s, we provided landmark coverage of the birth of ASICs; we even had staff members design several ASICs. And in the 1990s, we were at the forefront of the Internet age, launching a Web site in 1995, and you can still access those archives today. Design Ideas, a department that remains incredibly popular with readers, has been a part of *EDN* since the very first issue.

The 25th-anniversary issue has been a joy to review. Contributors—both *EDN* staffers and participants from the industry—proved remarkably savvy in looking forward. We've run several excerpts as examples. The predictions included broadband networks to the home and the convergence of computers, communications, and consumer electronics. Here's an example:

"Where will we be in 25 years? The availability of inexpensive computing will have considerable impact. Many more functions will be performed by digital computers. Voice communication over expensive media (wire, mobile radio) will occur digitally to save bandwidth and improve privacy via encryption. Many control functions within our household appliances and motor vehicles will be performed by digital computers because the more intelligent control they offer will utilize expensive resources more efficiently."—ME Hoff, Intel Corp, *EDN*, Oct 14, 1981.

We will choose milestones from our 50-year history that were important when they first occurred and that, even after five decades, still have an effect on key technologies.

We will share more of that 25th-anniversary issue with you throughout the remainder of 2006. Meanwhile, please let me know of any milestones that you think should be on the list. If there is a technology visionary that you'd like to hear from, let me know. EDN

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Apples and Oranges Working Together... That's the Power of Windows Embedded

The developers at Fujitsu know that the hundreds of peripheral drivers included in the Windows® CE operating system provide the solutions they need to easily integrate multiple device functions.

Needing to incorporate drivers for an infrared receiver, 802.11g WiFi card, and touch screen, the Fujitsu U-Scan Shopper development team chose Windows CE. Because Windows CE offers familiar, yet easily customized components and tools, they were able to develop the device in only five months. With the power of Windows CE, the Fujitsu U-Scan Shopper offers users coupons on demand, infrared scanners for product promotions, and in-store order placement, all from the convenience of the produce section, or wherever your shopping cart takes you.

We considered Linux, but couldn't have achieved the same results, so we chose the Windows CE operating system."

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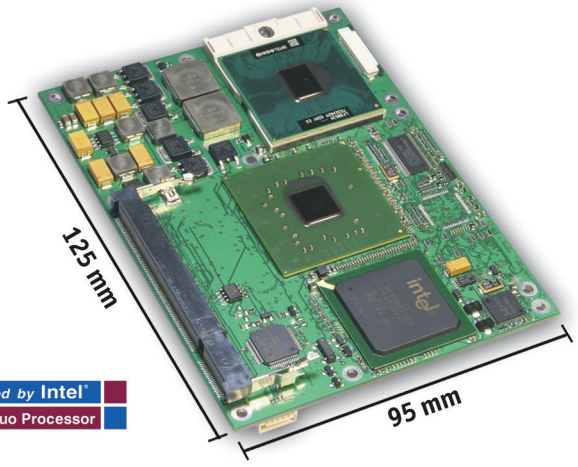

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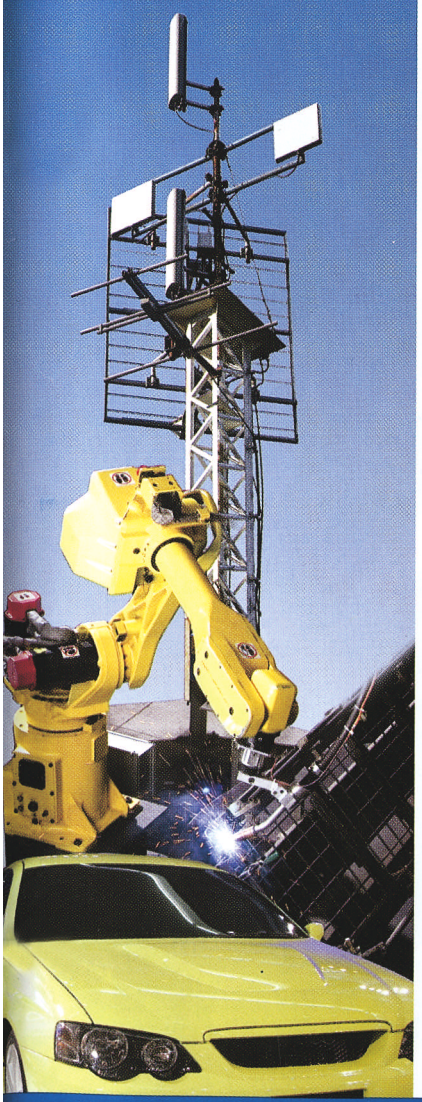


Buck Regulator Topologies for Wide Input/Output Voltage Differentials

— By Bob Bell, Applications Engineer and David Pace, Design Manager

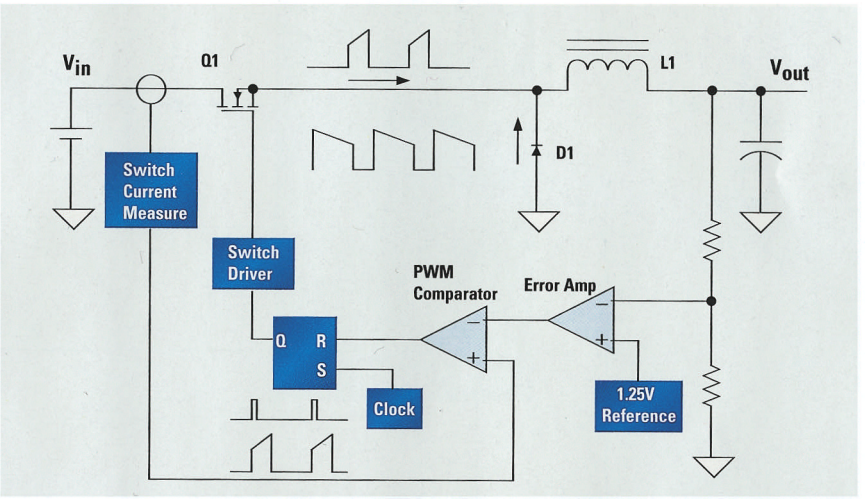


Figure 1. Buck Regulator Using Current-Mode Control

Buck regulators are used to efficiently step down a higher level, unregulated input voltage to a regulated output voltage. In applications requiring DC-DC conversion from a high input voltage, the buck regulator dramatically improves conversion efficiency relative to linear regulator alternatives. However, applying the buck regulator to applications with high input-to-output step-down ratios creates significant challenges for the pulse-width modulation (PWM) controller. Because the duty cycle of the buck regulator switch is approximately equal to V_{OUT}/V_{IN}, a buck DC-DC converter with high input/output voltage ratio must control very narrow PWM pulses. The switching frequency of a buck regulator is generally set to a high level to reduce the size of the inductor and capacitors. High switching frequency and low duty cycle translates to very short pulse durations in the controller. For example, a buck regulator with an input voltage of 66V and an output voltage of 3.3V will require a buck switch duty cycle of approximately 5%. At a typical switching frequency of 300 kHz, the required PWM on-time of the buck switch is a mere 166 ns.

Control methods or topologies used in buck regulators include Voltage-

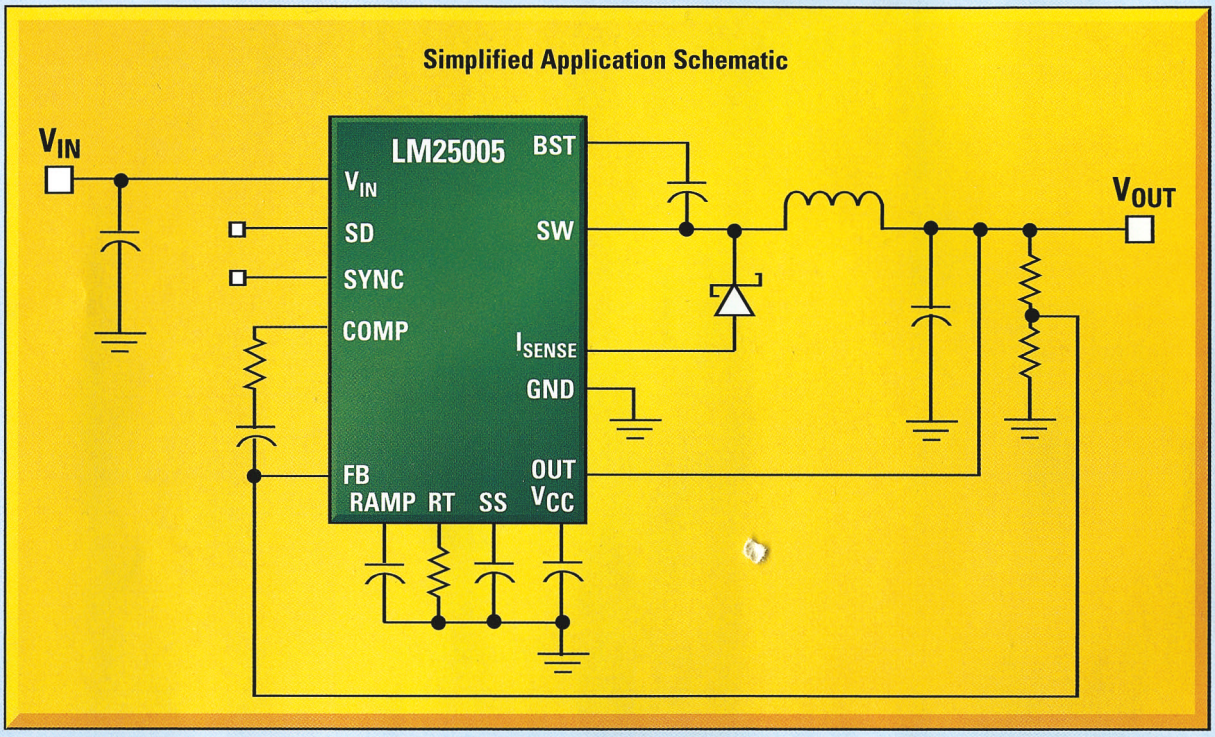
NEXT ISSUE:

Trade-offs in Synchronous Design

National Semiconductor

Integrated 42V, 2.5A Buck Switching Regulator

National's LM25005 With Emulated Current-Mode Control Reduces Noise Sensitivity and Enables Reliable Control of Small Duty Cycles at High Input Voltages



LM25005 Features

- Ultra-wide V_{IN} from 7V to 42V, supports load currents up to 2.5A
- Adjustable output voltage from 1.225V
- 1.5% feedback reference accuracy
- Current mode control with emulated inductor current ramp
- Programmable switching frequency with bi-directional synchronization capability simplifies system design
- Simulation support available
- Available in TSSOP-20EP (Exposed Pad) packaging AVAILABLE LEAD-FREE

Ideal for use in consumer electronics, telecommunications, data communications systems, automotive power systems, and distributed power applications

Product Highlight:

Allows multiple devices to self-synchronize or synchronize to an external clock

LM5005 High voltage version allows 75V max input voltage

For FREE samples, datasheets, and more information, visit www.national.com/pf/LM/LM25005.html

Buck Regulator Topologies for Wide Input/Output Voltage Differentials

Mode (VM), Current-Mode (CM), Hysteretic, and Constant-On-Time (COT) control. Current-mode control provides ease of loop compensation, FET switch protection, and inherent line feed-forward compensation. This makes current-mode control a favorite among power designers.

Hysteretic and Constant-on-Time controllers respond more quickly to load transients but do not operate at constant switching frequency. Constant-on-Time, a variant of hysteretic control, provides improved stability and less variation in switching frequency.

Current-Mode Control

Buck regulator ICs intended for high input/output step-down ratios must provide robust noise immunity when operating with very narrow duty cycles. In a current-mode topology, the challenge is the measurement and scaling of the inductor current. ***Figure 1*** shows the block diagram of a current-mode buck regulator. The output voltage is monitored and compared to a reference, with the error signal applied to the PWM comparator. The modulating ramp is a signal proportional to the buck switch current. When the buck switch is turned on, the inductor current flows through it with a slope of $(V_{IN} - V_{OUT}) / L$. An accurate, fast measurement of the buck-switch current is necessary to create the PWM ramp signal.

Propagation delays and switching transients makes it difficult to use current-mode control for large conversion ratio applications where very small on-times are required. Even with the best design practices, current sense and level shift circuits will add significant propagation delay. In addition, when the buck switch turns on, the reverse recovery current into the free-wheeling diode (D1) causes a leading-edge current spike with an extended ringing period (See ***Figure 2***.) This spike can cause the PWM comparator to trip prematurely. Attempts to filter or blank this leading-edge spike reduces the minimum controllable on-time of the buck switch.

Emulated Current-Mode Control

The challenge of accurate and fast current measurement can be met with a new proprietary method that emulates the buck switch current without actually measuring the current. The buck-switch current waveform can be broken down into two parts—a base, or pedestal, and a ramp. The pedestal represents the minimum (or valley) inductor current level. The inductor current falls to its minimum just before the buck switch turns on. A sample-and-hold measurement of the free-wheeling diode current, taken just prior to the turn-on of the buck switch, can capture the pedestal current information.

The other part of the buck-switch current waveform is the positive ramp to the peak level. The ramping current slope is described by, $di/dt = (V_{IN}-V_{OUT}) / L$. A signal equivalent to the current ramp can be created with a current source proportional to $V_{IN}-V_{OUT}$ and a capacitor (C_{RAMP}). If the current source (I_{RAMP}) is controlled by the difference between the input and output voltages, the capacitor charging slope is: $dv/dt = K^* (V_{IN} - V_{OUT}) / C_{RAMP}$, where K is a constant scale factor for the current source. The value of C_{RAMP} can be selected to set the capacitor voltage slope proportional to the inductor current slope.

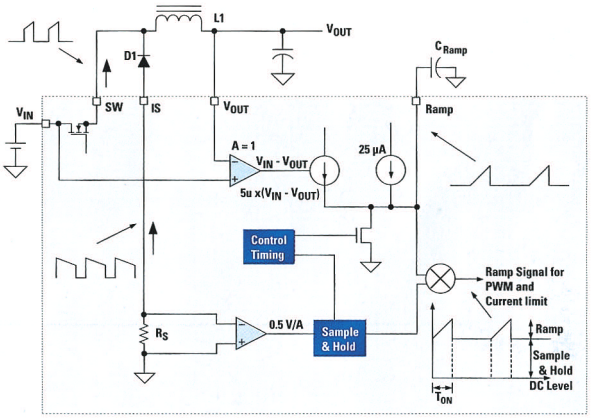
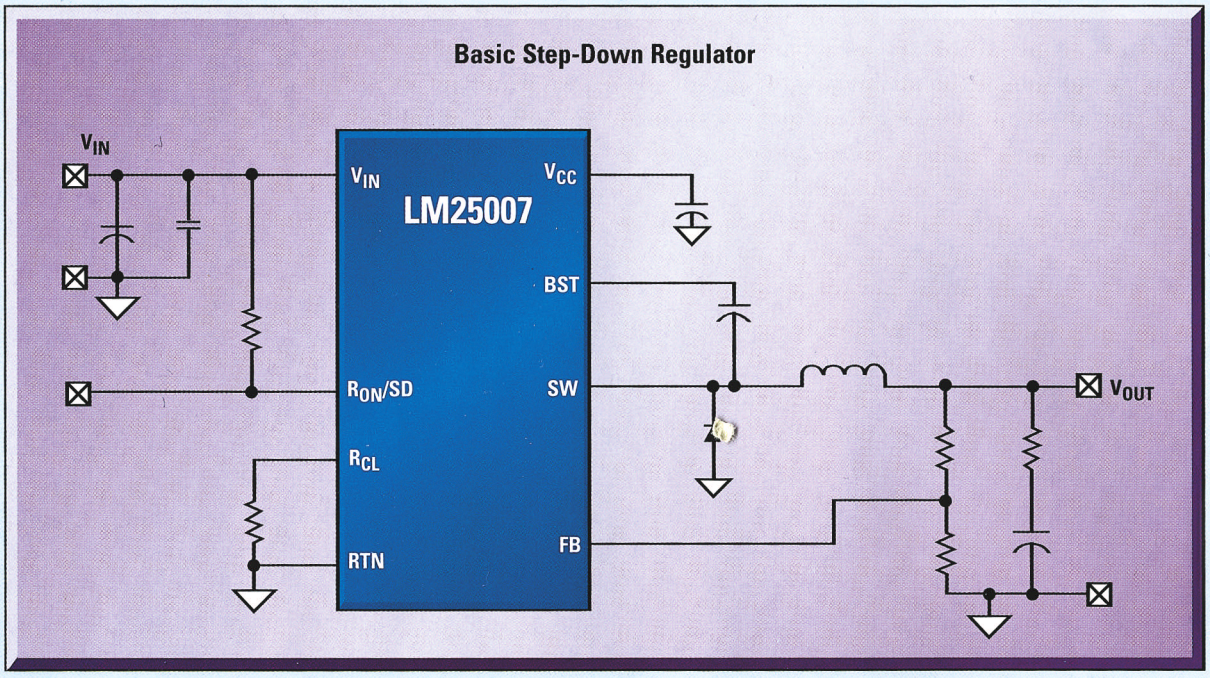


Figure 2. Emulated Current-Mode Regulator

Figure 2 presents the block diagram of the LM25005, an integrated buck regulator that implements the emulated current-mode control scheme described above. The free-wheeling diode anode is connected to ground through the

Highly Integrated 42V, 0.5A Buck Switching Regulator

LM25007 Has Constant-On-Time Architecture with V_{IN} Feed-Forward, Provides Ultra-Fast Transient Response, and Needs No External Components



LM25007 Features

- Wide V_{IN} from 9V to 42V, supports load currents up to 0.5A
- Ultra-fast transient response, reduced filter capacitance
- Up to 800 kHz switching frequency
- Precise DC current limit
- ±2% accurate, 2.5V feedback from -40° to 125°C
- Integrated high voltage bias regulator
- Available in thermally enhanced MSOP-8 and LLP packaging

AVAILABLE LEAD-FREE

Ideal for use in automotive electronics, telematics, Industrial systems, consumer electronics, distributed power supplies, high-voltage post regulators, industrial power supplies, and high-efficiency point-of-load (POL) regulators

Product Highlight:

V_{IN} feed-forward provides near constant operating frequency

LM5007 High input voltage version allows 75V max input voltage

For FREE samples, datasheets, and more information, visit www.national.com/pf/LM/LM25007.html

Buck Regulator Topologies for Wide Input/Output Voltage Differentials

controller. A small-value, current-sense resistor and amplifier are used to measure the diode current. A sample-and-hold circuit captures the minimum level diode current just prior to the turn-on of the buck switch. Sampling the valley current, each cycle provides the pedestal portion of the emulated current sense signal.

The LM25005 senses the input voltage and the output voltage to generate a current source that charges an external ramp capacitor (C_{RAMP}). When the buck switch is turned on, the capacitor voltage rises linearly during each cycle. When the buck switch is turned off, the capacitor is discharged. For proper operation, the ramp capacitor is chosen in proportion to the value of the buck inductor. The LM25005 sums the sampled current pedestal and the external ramp capacitor voltage and applies this signal to the PWM comparator. The final result is a controller that behaves like a peak current-mode controller but without the delay and transient effects in the current sensing signal.

For applications operating with duty cycles greater than 50 percent, peak current-mode controllers are subject to sub-harmonic oscillation. Oscillation is normally avoided by adding an additional fixed slope ramp to the current-sense signal (slope compensation). In the LM25005, an additional fixed offset current provides an additional fixed slope to the ramp capacitor signal. For very high duty cycle applications, the ramp capacitor value can be decreased to further increase the ramp slope and prevent sub-harmonic oscillation.

LM25005 output overload protection is accomplished with a dedicated current-limit comparator which limits the emulated peak current on a cycle-by-cycle basis. The emulated current-mode method provides the added benefit of capturing inductor current information prior to the buck switch turn-on. If the current pedestal exceeds the current-limit comparator threshold due to an extreme overload condition, the buck switch skips cycles to prevent current runaway.

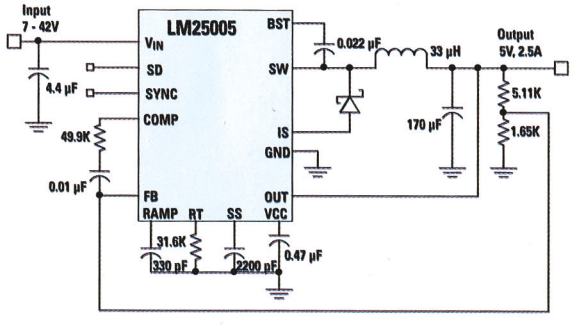


Figure 3. LM25005 Buck Regulator Schematic

Figure 3 shows an LM25005 controlled buck regulator designed for an input voltage range of 7V to 42V and an output voltage of 5V with a maximum load of 2.5A.

Constant-On-Time Control

Another solution involving high input/output ratio buck regulators is Constant-On-Time control. This method can be thought of as a gated one-shot, where a feedback comparator triggers the next buck switch on-time when the output voltage falls below a threshold level. COT control is well suited for applications with high input/output voltage ratios because the one-shot can be programmed for a very short on-time and the feedback comparator will adjust the off-time to achieve the necessary low duty cycle. The noise sensitivity of a PWM ramp operating at low levels are completely eliminated. The COT technique has been used for many years for simple, cost-effective DC-DC converters because it requires no error amplifier or loop compensation components. The central issue of this method is frequency variation with input voltage and the possibility of sub-harmonic oscillation.

The block diagram in *Figure 4* illustrates the LM25010, a new member of a generation of COT buck regulators that solves these problems. The one-shot which controls the on-time is programmed by resistor R_{ON} which is connected between the unregulated input voltage and the controller. The period of the one-shot (T_{ON}) thus varies inversely with the input voltage. Using the simplified equation for the duty cycle (D) of a buck regulator, with Fs representing switching frequency:

$D = V_{OUT}/V_{IN}$

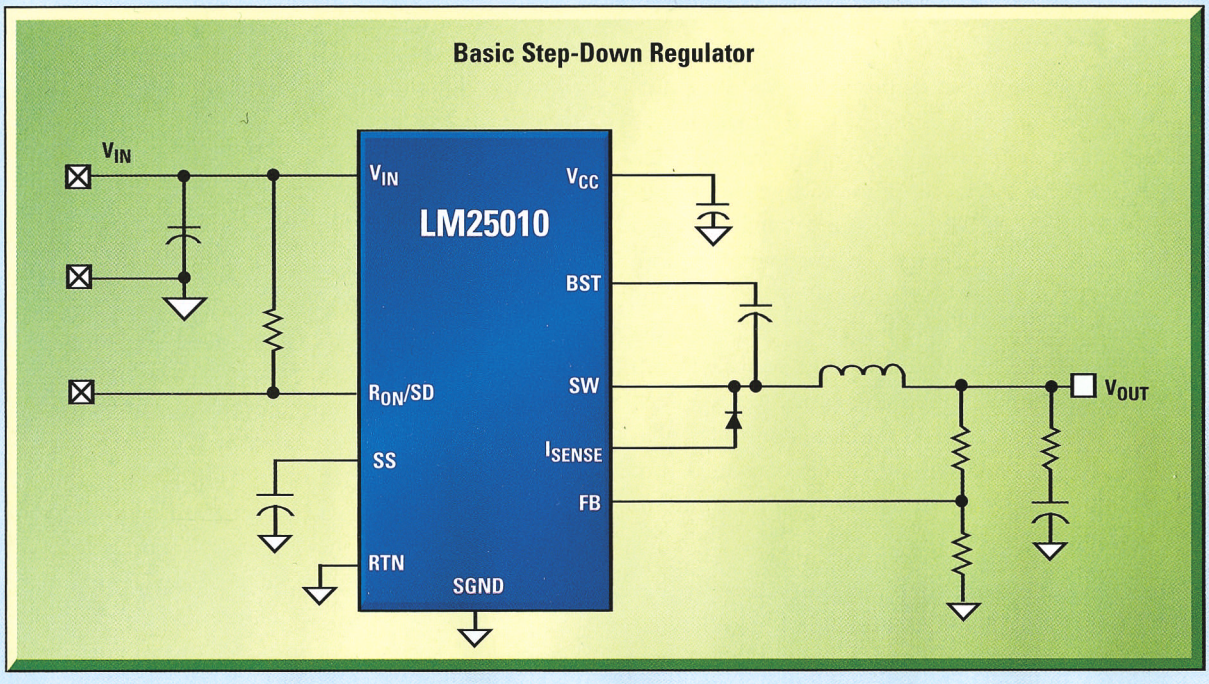
But by definition, $D = T_{ON}/(T_{ON}+T_{OFF}) = T_{ON}*Fs$

Since, $T_{ON} = K/V_{IN}$

Therefore, $Fs = V_{OUT}/K$

Highly Integrated 42V, 1.0A Buck Switching Regulator

LM25010 With Constant-On-Time Architecture and V_{IN} Feed-Forward Provides Ultra-Fast Transient Response and Near-Constant Operating Frequency



LM25010 Features

- Wide V_{IN} from 6V to 42V, supports load currents up to 1.0A
- Ultra-fast feed-forward response, modulated filter capacitance
- Switching frequency up to 1 MHz
- Valley current limiting at 1.25A
- ±2% accurate, 2.5V feedback from -40°C to 125°C
- Integrated high voltage bias regulator
- Available in exposed pad LLP-10 and TSSOP-14 packaging

AVAILABLE LEAD-FREE

Ideal for use in non-isolated telecommunications, secondary-side post regulators, and automotive electronics

Product Highlight

No control-loop compensation required

LM5010 High input voltage version allows 75V max input voltage

For FREE samples, datasheets, and more information, visit www.national.com/pf/LM/LM25010.html

Buck Regulator Topologies for Wide Input/Output Voltage Differentials

Thus in any application where the desired V_{OUT} is a fixed value, the on-time can be programmed to achieve a desired switching frequency and the frequency will not vary significantly with changes in the input voltage.

One challenge associated with COT regulators is current limiting. If the on-time is terminated by a current-limit circuit which senses the current in the buck switch, the output voltage will fall and the off-time will decrease to its minimum value in an attempt to maintain voltage regulation. The frequency of the regulator will increase to an extremely high value, limited only by the propagation delays, and power dissipation within the IC will become excessive. Some buck regulator solutions arbitrarily enforce a minimum off-time after current limit is detected to guarantee that the frequency does not increase excessively in overload conditions. This approach produces a fold-back in the current limit I vs V characteristic which can limit the useful load range of the regulator.

The LM25010 illustrated in ***Figure 4*** solves the current limit dilemma with a simple yet effective method. The free-wheeling diode current is routed through a sense resistor in the IC. The current in the diode is sensed by a resistor and monitored by a comparator. If the current flowing through the free-wheeling diode exceeds the current-limit threshold, the current-limit comparator will disable the buck switch until the diode current falls to an acceptable level. The off-time is automatically increased to the time required for the buck inductor current to ramp down to the desired valley current. Thus, neither the output current nor the switching frequency can run away during overload.

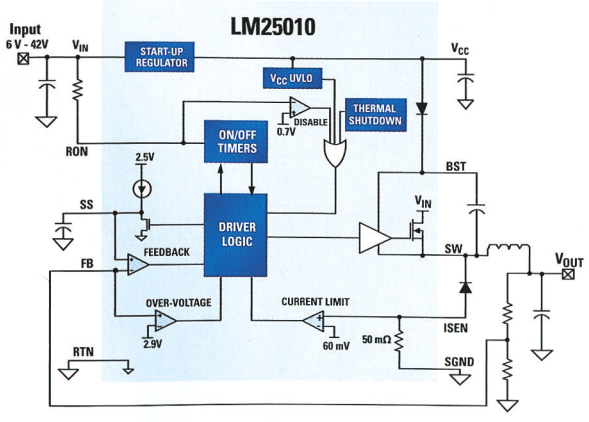


Figure 4. LM25010 COT Buck Regulator

Regulators based on COT control are subject to erratic switching behavior if there is not sufficient ripple voltage present at the Feedback (FB) pin. If the output capacitor has a large enough Equivalent Series Resistance (ESR) this issue can be avoided. In applications where a relatively large output ripple cannot be tolerated, several ripple reduction techniques are available.

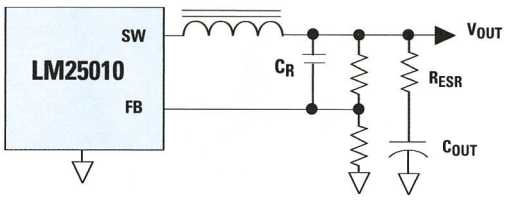


Figure 5a. COT Ripple Reduction Using C_R

In ***Figure 5a***, the ripple at V_{OUT} is fed to FB through C_R. Therefore the ripple at V_{OUT} can be less than in the standard circuit since it is not attenuated as much by the feedback resistors.

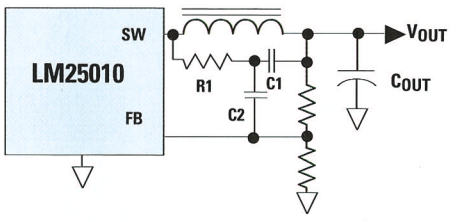
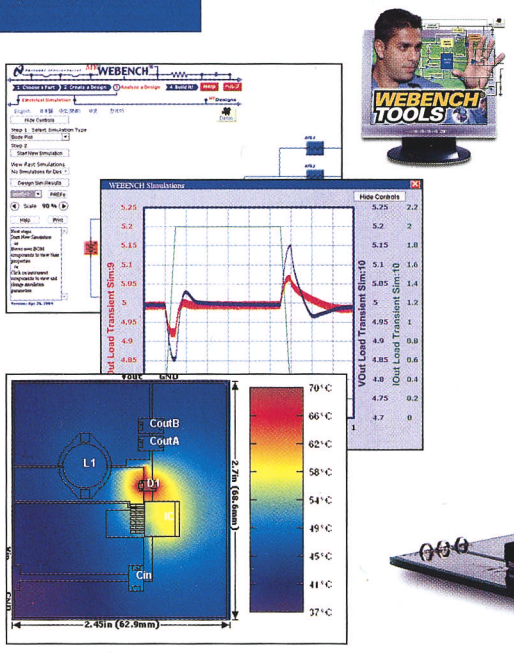


Figure 5b. COT Ripple Reduction Using R_1,C_1, and C_2

In ***Figure 5b***, the R_{ESR} is removed resulting in low ripple at V_{OUT}. The ripple required at FB is produced by R_1, C_1, and C_2. Since V_{OUT} is an AC ground, and the SW pin switches between V_{IN} and ground, a sawtooth is generated at the R_1, C_1 junction. C_2 then couples that ripple to FB.

These are some of the control methods and topologies favored by power designers. For more information on high-voltage switching power supply topologies, visit www.national.com/onlineseminars. ■

Power Design Tools



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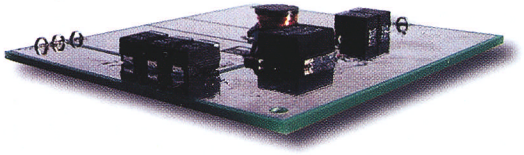

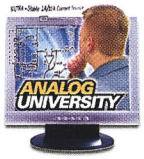

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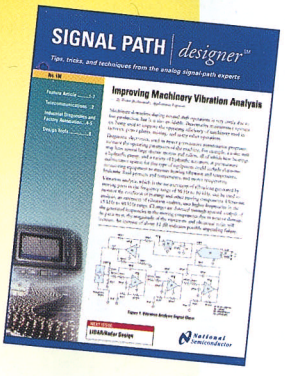
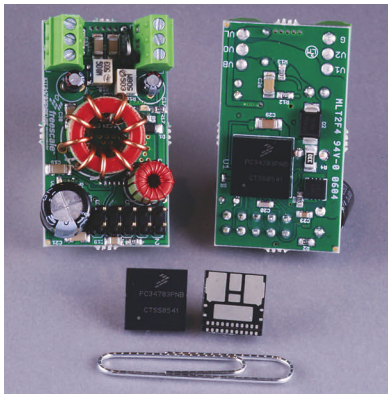


National Semiconductor

550263-011

Power-management IC suits advanced microprocessors' power needs

Although Freescale tailored the MC34703 Quiccsupply 3, the newest member of the Quiccsupply power-management family, to fit into the PowerQuicc III line of telecom and networking processors, it's equally well-suited to other vendors' processors, according to Freescale Systems and Application Engineer Lonne Mays. "Many of today's advanced processors have both a core supply and an I/O supply that have requirements for how they track each other as they power up or down," he says. "With Quiccsupply, you can set the appropriate sequence for that processor." The device has a synchronous buck regulator for core voltages, providing current as high as 10A and a low-dropout controller for power I/O and bus voltages for current as high as 2A.



The Quiccsupply 3 power-management-IC evaluation board (top) follows the trend of combining several circuits onto one MCM (middle). The device provides currents as high as 10 and 2A.

The device follows the trend of other recently introduced power controllers of combining several circuits onto one MCM (multichip module) but stops short of packing all external components into the device. "We keep the magnetics and other components external to gain flexibility," says Mays. "For example, if you need 5 rather than 10A, you could substantially shrink the magnetics and power supply."

The device switches nominally at 300 kHz but is adjustable from 200 to 400 kHz. Input voltages are 2.8 to 13.5V. The unit is available in a 10×10-mm, 33-lead PQFN package and sells for $3.75 (10,000). An evaluation board costs $100.30.**—by Margery Conner**

▷**Freescale Semiconductor**, www.freescale.com

Novas introduces on-the-fly debugging

Novas Software officials hope that the company's new product for on-the-fly debugging of IC code will prove to be as big a hit in the market as its Debussy and Verdi products are. Novas President and Chief Executive Officer Scott Sandler says that the new offering, Siloti, allows Novas debugging tools to dump signals on the fly during simulation and emulation without stopping the simulation or emulation. In today's SOC (system-on-chip)-verification environments, it is inconvenient and time-consuming to start and stop simulations and emulations to get signal dumps to run a debugger.

Siloti addresses this issue by taking what amounts to essential registers from the code on the fly to help the Debussy and Verdi tools get full visibility into signal behavior without halting simulation runs. Novas offers Siloti SimVE for simulation environments and Siloti SilVE for emulation, prototyping, and silicon debugging. The company claims that, for early customers of Siloti, the product provides a fourfold decrease in debugging with hardware emulation and improves design visibility fivefold when users deploy it with a design-for-debugging methodology, in which RTL designers identify critical signals before performing simulations. Before designers simulate a design, they feed RTL or gate-level source code to Siloti. The tool then analyzes the code to determine which registers need to provide full visibility.

In an emulation environment, the SilVE tool performs sampling and analysis, signal expansion, and subsequent debugging of the design code rather than performing them on the netlist of the FPGA. Sandler says Siloti expands only the sections that users want to examine, which means that the simulator or emulator needs to dump just those parts of a file a user wants to examine. The Siloti SilVE and SimVE each start at $65,000 for a one-year subscription.**—by Michael Santarini**

▷**Novas Software Inc**, www.novas.com.

Tools take asynchronous design mainstream

EDA and IP (intellectual-property) start-up Silistix has unveiled tools that it claims will free IC designers from slavery to a single system clock by allowing them to stitch together IC-design blocks with the company's asynchronous IP bus. Asynchronous design has thus far been a practical methodology only for advanced designers, but with its IP and EDA combo, Silistix believes it can make the methodology more accessible to mainstream ASIC and SOC (system-on-chip) designers. The company introduced itself and its Chain-fabric asynchronous-bus IP last December. Now, it is releasing the tools that implement the bus.

The ChainWorks flow comprises two tools that plug into the traditional ASIC/SOC-design flow and a library. The Chaindesigner graphical-entry tool helps users arrange IP and proprietary-logic blocks in their designs and then interconnect them to come up with a desired network topology. Users feed the tool Verilog, SystemVerilog, or SystemC, allowing them to define initiators and targets, as well as the ports for the initiators and targets, according to David Fritz, the company's vice president of marketing. He claims that users prefer the tool's GUI because it provides a more formal mechanism for visualizing, understanding, and designing the interconnect. A future version of the GUI will allow designers to embed notes in the design to better monitor progress and describe intent.

After users design a topology, the tool generates Verilog and SystemC models and testbenches for simulation, as well as constrained Chain netlists for input to Chaincompiler. After designers have verified their design topology, they can then use the Chaincompiler asynchronous-synthesis tool to implement the design, interconnecting the various blocks with the company's Chain-fabric bus. Chaincompiler uses the proprietary-asynchronous-interconnect Chainlibrary of components to produce the structural netlist. "Chaincompiler combines the library components to construct your interconnect network and then generate a structural netlist that goes into conventional logic-synthesis tools, such as Synopsys Design Compiler," says Fritz. It also generates static-timing-analysis scripts, place-and-route hints critical for self-timed circuits, and test patterns.

The first release supports scan insertion for interconnect ports, and a future release will include partial-scan BIST (built-in self-test). Users can run iterations between ChainWorks and synthesis, timing analysis, place and route, and extraction. However, most users need to go through the flow only once. The company believes that the flow will open asynchronous design to mainstream use, although it so far has no customer tape-outs to report. It has, however, developed a test chip in-house and claims that unnamed customers are using the tool on current projects.

—by Michael Santarini

▷**Silistix**, www.silistix.com.

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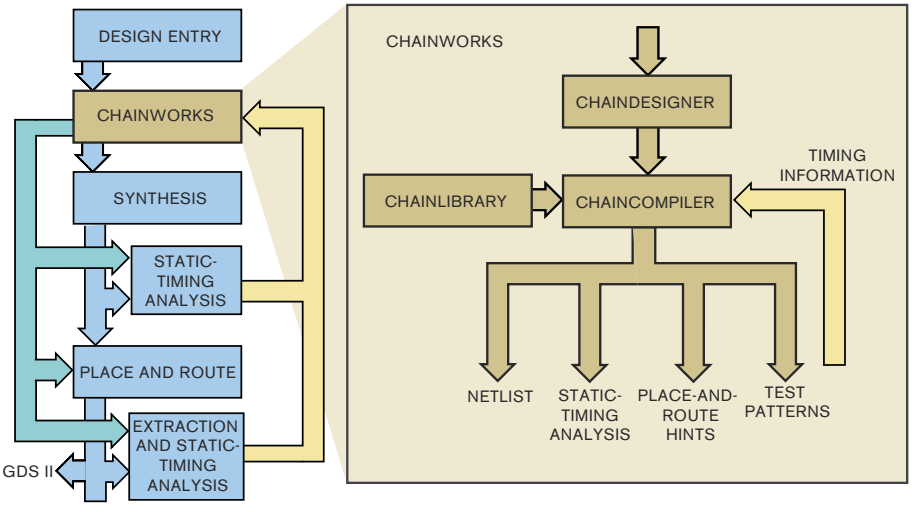

The ChainWorks flow comprises two tools that plug into the traditional ASIC/SOC-design flow and a library.

DILBERT *By Scott Adams*

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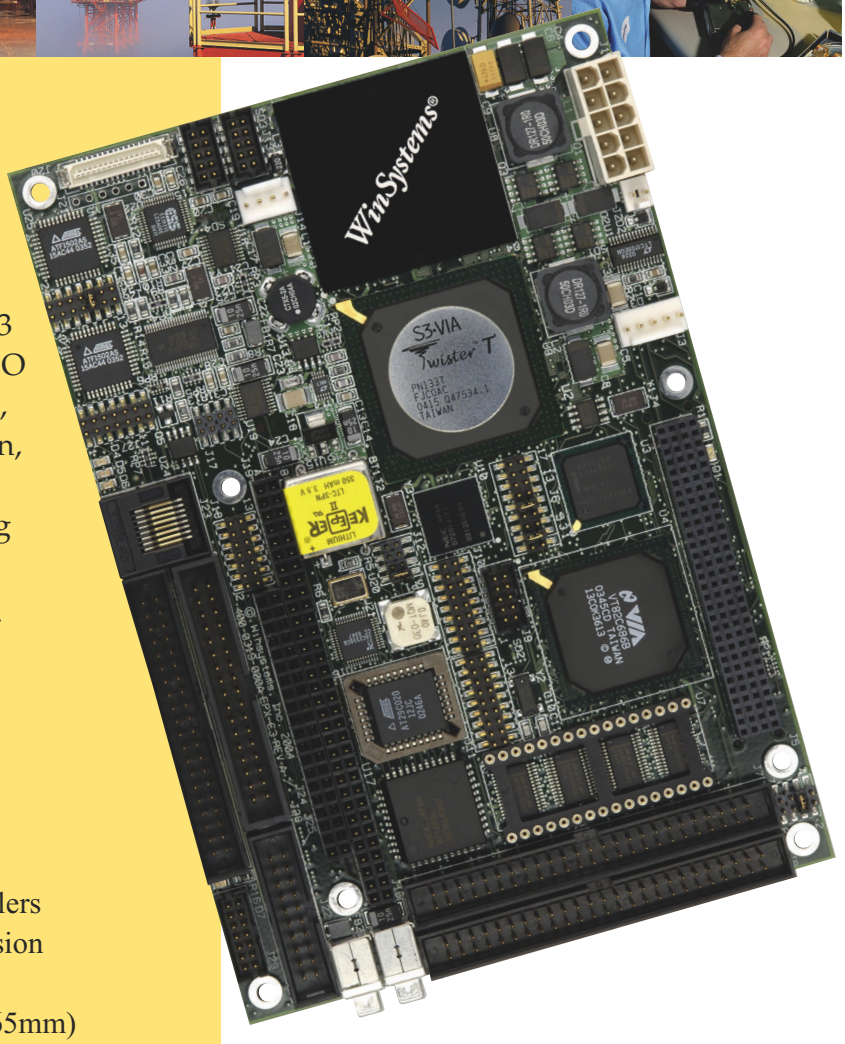

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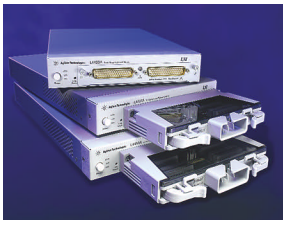
1U, half-rack switching units' debut kicks off supplier's LXI push

The proponents of LXI (LAN extensions for instrumentation), the Ethernet-based interconnect and packaging technology for test-and-measurement products, are confident that LXI overcomes the most serious shortcomings of card-cage-based modular approaches, such as PXI and the older and larger VXI. Moreover, advocates believe that LXI is the first modular-instrument technology that works equally well on the benchtop and in test-and-measurement systems. Agilent, one of the companies that led the way in developing LXI, is now among the first to offer LXI-based products. Agilent based the seven new, 1U (1.75-in.)-high, half-rack-width L4400-series modules on plug-in cards for the vendor's eight-slot 34980A modular switch/measure mainframe, which is now also LXI-compatible. The new units enable smaller, lower cost configurations for systems that don't need eight plug-in cards and can benefit from locating the signal-switching functions inches away from the unit under test.

Each unit surrounds its card with a protective shell that also houses an ac-line-operated power supply. The seven units



The 1U-high, half-rack-width switching and data-acquisition units in the LXI-based L4400 series suit applications that need fewer than eight cards and can benefit from placing the system inputs and outputs close to the unit under test.

are a 40-channel armature-relay multiplexer; a four-by-eight-point reed-relay matrix; a 32-channel general-purpose switch; a microwave switch with an external attenuator driver; a 64-bit digital-I/O unit with memory; a four-channel DAC with memory; and a multifunction unit with 32 digital-I/O points, two DACs, and a counter. Prices for these units range from $1506 to $2709. The company also offers a $350, rack-mountable shelf, which can house one or two half-rack-width LXI units, including units that are taller than the 1U-high L4400-series products.

The units' graphical-interface software supports the L4400 series and the 34980A. According to the company, this software, which you can operate remotely through a LAN-connected computer with a standard Web browser, goes well beyond the requirements of the LXI standard. The password-protected, operating-system-independent software enables setup, debugging, and troubleshooting of signal-switching systems, including checking configurations; opening, closing, sequencing, and monitoring switches; and sending and capturing SCPIs (standard commands for programmable instruments). The software incorporates an I/O analyzer that lets you examine the error queue and provides status reports that include calibration status and a count of the number of times each relay has operated. You can try out an interactive demo of the software at www.agilent.com/find/L4400.

—by Dan Strassberg

▷**Agilent Technologies**, www.agilent.com/find/L4400.

Chip improves efficiency of flyback-converter circuits

Secondary-side SR (synchronous-rectification) circuits in high-power-flyback- and half-bridge-converter circuits have drawbacks: They can be difficult to design, and they may be subject to patent and licensing restrictions. In addition, their use of a current-transformer circuit to sense polarity changes in the rectifying MOSFETs results in a large, energy-wasting, unused current that oscillates between the transformer and the output-filter capacitor.

The IR1167 SmartRectifier IC directly and precisely senses the voltage threshold across the SR MOSFET.

Addressing these issues, International Rectifier's new IR1167 SmartRectifier IC directly and precisely senses the voltage threshold across the SR MOSFET. The company claims that the chip can increase system efficiency by 1% by halving the losses the MOSFET dissipates and reducing the MOSFET's temperature by 10°, thus reducing the number of MOSFETs or allowing a change in part size from TO-220 to SO-8 packages. The device is also available in DIP-8 packages.

The SmartRectifier works with the IRF7853, the IRFB4110, and the IRFB4227 MOSFETs, which feature low on-resistance and gate-charge characteristics. The device sells for $1.08 (10,000).**—by Margery Conner**

▷**International Rectifier**, www.irf.com.

FROM THE VAULT

By 2006, then, the television, which we think of today as our window on the world, will fill a much, much larger position in our lives. Of course, the TV itself will evolve dramatically from a mere display device, becoming an intelligent two-way medium that combines telephone, television, and computer. It will control appliances (even robots) in the home; do our bookkeeping; compute our taxes; buy and sell stocks; make airline, hotel, and theater reservations; teach and entertain us; enable us to work at home; and even give us advice. And it will provide all of these functions at a reasonable price.

Thomas J Lonergan, president and co-founder, Wolfdata Inc, *EDN*, Oct 14, 1981.

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VOICES

Economies of Freescale

Michel Mayer, chairman and chief executive officer of Freescale Semiconductor, discusses his company's future, the shift to low-power processors, and the source of future competition. An excerpt of that interview follows. You can find the complete interview at www.reed-electronics.com/electronicnews/article/CA6308384.

Do you see a shift in the processor market toward multiple processors rather than a single extremely powerful processor?

A Yes. I am completely convinced of that [scenario]. The center of innovation is moving away from the PC and IT. There will always be a market for faster, CMOS-core processors. But, frankly, the bulk of the market is going to distributed processing and low power. Intel [www.intel.com] essentially accepted that premise and said that multicore is the way to go. But, even beyond that, there will be a whole set of more efficient, low-power processors.

Will they be general processors or custom processors?

A The architectures will be general, whether it's ARM [www.arm.com] or PowerPC or some simpler types. I believe the change will be in the applications. More types of SOCs [systems on chips] will include these processors.

Who becomes your chief competition in this market, assuming that it's neither AMD [www.amd.com] nor Intel?

A Over time, Intel and AMD will have to branch out. In the cell-phone and the portable areas, it is still TI [www.ti.com], Philips [www.Philips.com], and STMicroelectronics [www.st.com]. A few companies have multimedia consumer applications. And, of course, in DSPs, TI has some. In the automotive industry, that's more Microchip, NEC, Renesas, and Infineon with its TriCore [www.microchip.com, www.necel.com, www.renesas.com, www.infineon.com]. More and more companies are using ARM, which is more of a general processor that finds use across segments. We believe our PowerPC will play an important role in embedded processors.

Will it be a volume game, in which you produce in huge quantities, or will it be about specialization?

A Some applications are high-volume by themselves. Whether or not you have a completely custom solution, they are already in high volume. A case in point is gaming. The gaming processors, whether Playstations or Xbox 360s, are fully customized. If they're completely customized and not high-volume, you have to be generic. By the way, even Intel wasn't completely successful in the general-processor space. It was highly successful in one application: the PC. It's difficult to take a PC processor and branch out. There's not a lot of customization you can do. So, to answer your question, things will need to remain customized. What's happening as we evolve is that with SOC techniques and mix-and-match IC libraries, it makes it possible for those segments to share more.

What effect does a combination of commonality and customization have on your costs at advanced architectures?

A It's not only a problem with processors. It's a problem with the whole SOC.

Typically, the only way to offset that problem has been with high volume.

A There are several ways to achieve high volume to offset your R&D. One is to have better IP [intellectual-property] reuse—better commonality. That's the wave of the future. A lot of key players are developing design strategies that allow you to more easily reuse such things as communication blocks, because everyone now needs to access the Internet. The design techniques will evolve to be more flexible. Otherwise, you cannot solve your R&D dilemma.

What effect has the Crolles Alliance with Philips and STMicro had on your R&D costs?

A Anything that helps develop some of the common processes is good. Partnerships are now becoming increasingly important in this industry. Crolles is one of the most publicized, but we have a lot of other partnerships in IP and joint developments with our customers and partners. We've been focusing a lot on process development and manufacturing and the need to have critical mass to remain as an IDM [integrated-device manufacturer]. The need to have a broad portfolio of IP to be able to offer multifunction SOCs and mix of analog and digital functions will be drivers for consolidation. It's not just at the IDM level. A lot of companies are going to have to either be good at partnering or be integrated.

Do you see any shift in where your products are ending up?

A Assembly and test are happening in Asia, but there are still wafer fabs in the United States and, to a lesser extent, in Europe. The foundry work is occurring in Asia. AMD is investing in Dresden, Germany. Intel is in the United States.

You've now been at Freescale since mid-2004, which is enough time to really understand the company. What's your biggest challenge?

A Getting enough talent. We're making great progress along those lines, but it continues to be a challenge. Also, changing the culture of the company. We have a lot of challenges: the market, the technology, the manufacturing. If I can bring in the same kind of talent that I've brought in so far, if we can change the culture, we can do great things.

–by Ed Sperling, Editor in Chief, *Electronic News*

Blackfin is action packed

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- IP TV
- Mobile TV
- Telepresence
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- ▶ **Streaming Media**
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The V300 Portable Media Player needed a processor that could enable 8 hours of MPEG-4 or MJPEG video playback and 16 hours of MP3 music, and run its operating system and application set. After auditioning a long list of prospects, Blackfin® got the role. Why? Blackfin easily met the V300's performance goals while powering the system from a 600 mAh battery. Then Blackfin nailed the part with $5 to 1200 GMACS scalable performance for content and applications.

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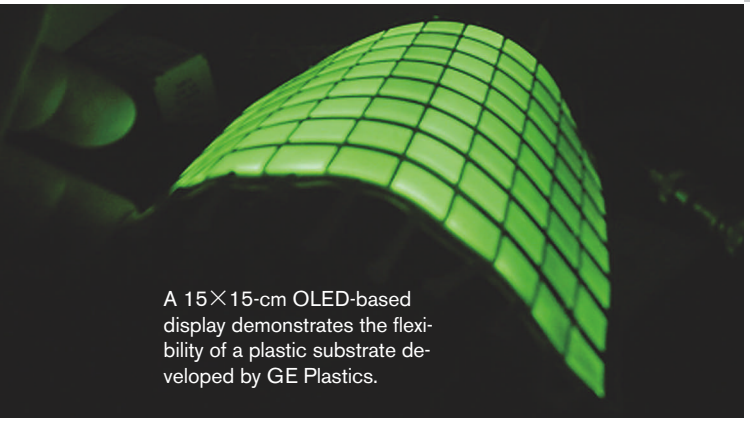


A 15×15-cm OLED-based display demonstrates the flexibility of a plastic substrate developed by GE Plastics.

RESEARCH UPDATE

BY MATTHEW MILLER

Plastic substrate allows OLED displays to get bent

Researchers at GE Plastics have detailed a plastic-substrate system that they claim will lead to OLED (organic-light-emitting-diode)-based displays that are more flexible, lighter, more durable, and less costly to build than those based on glass substrates.

The system combines a high-temperature Lexan polycarbonate film with a transparent coating that protects the display from oxygen and moisture. The high clarity and high temperature resistance of the Lexan film enable the construction of a 125-micron-thick substrate that can withstand the heat involved in OLED fabrication and still allow optimal light transmission, according to the company. In addition, the system should be amenable to high-volume-manufacturing processes that will drive down cost.

▷**GE Plastics**, www.geplastics.com.

Nanotube-based ultracapacitors could rival batteries

Researchers at the Massachusetts Institute of Technology (Cambridge, MA) report that an electrode structure based on a matrix of vertically aligned carbon nanotubes could drastically improve the energy density of ultracapacitors. Whereas the energy density of commercial ultracapacitors tops out at 6 Whr/kg, a nanotube-based version could offer 60 Whr/kg—comparable to lithium-ion batteries, the researchers claim. Meanwhile, such a device could provide power density of 100 kW/kg—three orders of magnitude better than lithium-ion batteries—and 300,000-cycle durability. For more information, go to http://web.mit.edu/newsoffice/2006/batteries-0208.html.

▶**Massachusetts Institute of Technology**, www.mit.edu.

03.30.06

Standard silicon conjures continuous laser

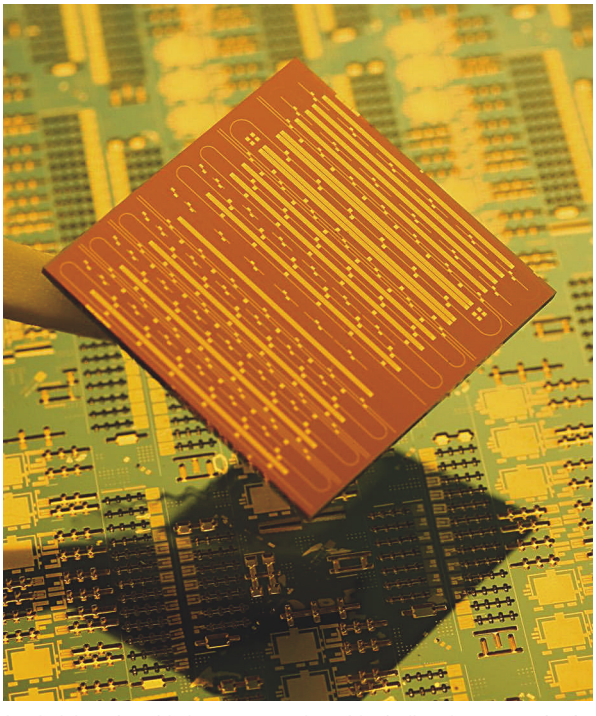
Intel researchers claim to have attained a significant industry first: a continuous-wave laser that the company built using a standard silicon-manufacturing process. The advance could lead to a new generation of low-cost lasers that designers could integrate with standard electronics for applications in high-speed interconnect and medical devices.

The 15×15-mm chip routes light from an external source through an S-shaped waveguide that's etched into the silicon and coated with a reflective thin-film material. Natural atomic vibrations in the silicon amplify the light in the well-known Raman-effect phenomenon, which is 10,000 times stronger in silicon than it is in glass fibers.

In addition, the researchers employ a PIN-semiconductor structure to mitigate the two-photon-absorption effect, in which two photons from the light source collide with an atom within the waveguide, knocking free an electron. The PIN structure acts as a "vacuum" that prevents these excess electrons from accumulating and absorbing so much light that the laser stops functioning, according to the company.

Visit the Web version of this article at www.edn.com/060330ru1 for a link to additional background, including video, animation, and coverage from the journal *Nature*.

▷**Intel Corp**, www.intel.com.



Intel claims that this laser-generating chip, built using a standard silicon process, could drive low-cost, diminutive lasers into applications including high-speed, on-chip interconnect.

Blackfin is picture perfect

▶ Leica Digital-Modul-R digital back for analog SLR cameras

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- Biometrics
- Driver Assistance
- Streaming Media
- High Definition
- Effects Processing
- Triple Play
- ▶ **Image Processing**
- VoIP
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- Baseband Processing
- Digital Radio
- Global Positioning
- Packet Processing
- GCC/Linux
- Cryptography
- Rights Management
- Open Source
- Car Telematics
- IP TV
- Mobile TV

10 megapixel image compression in ½ second

To equip professionals with a powerful and compact photography module for its analog SLR cameras, Leica Camera AG needed a small high performance processor. So the company focused on Blackfin's advantages. These included dual-processing cores up to 600 MHz that use just 144 mm^2 of board space, and Blackfin's ability to do Leica's color interpolation, auto exposure, auto white balance, gamma correction, and JPEG compression of 10 megapixel images. Smaller footprint, higher performance: No wonder Blackfin® is everywhere.

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ANALOG DEVICES

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DAQ chips simplify sensor interfaces

You can connect a wide variety of sensors to digital systems using austriamicrosystems' AS8500 and AS8501 chips to perform the analog-front-end and analog-to-digital-conversion function. The devices comprise a chopper input, a programmable-gain preamplifier, a 16-bit ADC, and a DSP filter block. They allow you to make direct connection to very-low-level sensor signals, such as low-value current-sense resistors or thermocouples, and operate from a single 5V supply. The chips offer resolution of less than 1 μV and linearity error below 0.1%, with sampling rates as high as 16 kHz. Applying correction in the digital section of the chip provides offset-free operation, and external averaging allows systems to achieve resolution of 21 bits. The chopper-input stage handles a maximum of four inputs, which you can use as single-ended, ground-referring connections or in pairs in a fully differential mode.

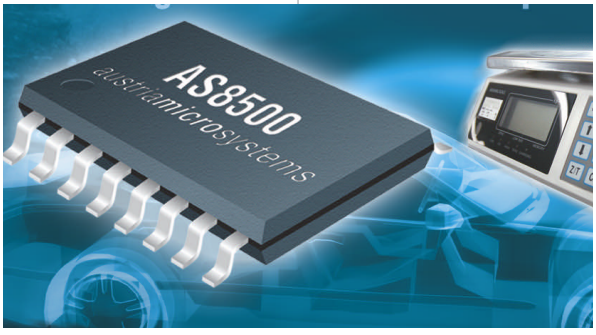
The company delivers the 8500 with a standard trim setting; for higher precision, the 8501 provides a calibration routine that characterizes each chip's functional analog parameters at final test and writes a set of trimming values into internal registers on the silicon. Internal-register settings also control the chips' configuration, and you can rewrite them at any time. The delivered default configuration is a read-only converter. Likewise, you set register values to select programmable gain of 6, 24, 50, or 100 to select full-scale measurement ranges of 7 to 120 mV. A three-wire serial interface outputs filtered digital data to a host system.

With austriamicrosystems' focus on mixed-signal design, the chip's designers gave particular attention to internal decoupling between analog and digital circuitry, part of a strategy to achieve low noise. Offset is less than 500 nV, and temperature-coefficient offset is negligible.

The chip also integrates a precision voltage reference, a temperature-measurement element, and a digital comparator. The parts operate over −40 to +125°C and suit use in automotive and industrial applications. To monitor current in a vehicle-battery lead, a 100-μΩ sense resistor provides measurement resolution of 10 mA in a full-scale range of 1500A. Self- and system-calibration routines run at power-up. The AS8500/1 chips sell for €5.50 ($6.60) and €6.60 ($7.90), respectively (1000).

—by Graham Prophet, *EDN Europe*

▷**austriamicrosystems**, www.austriamicrosystems.com.



With the AS8500/1 chips, you can build a complete low-noise, precision sensor-signal-conditioning front end to a microcontroller-based system.

Headphone amp swaps modes to cut noise, save power

03.30.06

Designers working with portable audio products have a new option in the constant trade-off of performance versus battery life: Wolfson's WM8985 audio codec. The device has a headphone-output stage that is dynamically switchable from operation in Class A/B to operation in Class D. Class A/B offers a conventional route to a high-quality, low-distortion output but requires a standing current through its output-stage devices and has a higher power demand. Class D has lower losses. A spokesman for Wolfson makes the subtle point that, in Class D, headphone driving is about power consumption rather than power dissipation.

Although manufacturers in recent years have greatly refined the quality of Class D amplifiers, designers may sometimes not want to use them. Class D is by definition a switching-output mode and introduces some level of harmonics and noise. In a device such as a smart phone with an MP3 player, designers may want it to operate in Class D when the RF section of the handset is not active and in Class A/B when it is. In handsets with FM radio, Wolfson notes, the headphone lead is also typically the FM antenna and cannot carry Class D-output waveforms while receiving FM.

Switching on the fly between modes, the codec can accommodate this requirement. At typical power outputs of 10 mW, switching to Class D reduces power consumption by approximately 50%. The 8985 also integrates a DSP for filtering and equalization, differential or line inputs, audio mixing, and a PLL that can accept a wide range of clock inputs. It has a switchable output and one that is in permanent Class A/B mode. SNR figures for the device's DAC, ADC, and headphone driver are 98, 92.5, and 90 dB, respectively. In standby mode, the device uses 360 μW.—**by Graham Prophet, *EDN Europe***

▶**Wolfson Microelectronics**, www.wolfsonmicro.com.

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RAMAC launched disk-drive revolution

Computers weren't new back in the fall of 1956. IBM developed the Mark 1 calculating machine in the 1930s, and researchers at the University of Pennsylvania completed the ENIAC (electronic numerical integrator and computer) in 1945. Many technology historians consider ENIAC the first successful general-purpose digital computer. But the 305 RAMAC (random-access-method-of-accounting-and-control) system, which debuted in September 1956, was the first to include near-line random-access storage in the form of the IBM 350 Disk File. Before the emergence of the Disk File, core, tape, and drum memory provided the only storage option.

The Disk File afforded access to effectively 4.4 Mbytes of data, for the first time making the real-time retrieval and manipulation of database records a reality. The Disk File featured 50 24-in. disks that stored 5 million 7-bit characters. At the product's launch, IBM claimed that, to realize similar capacity using drum memory, one would have had to use a 42-ft-long, 13-in.-diameter drum. IBM leased the 305 RAMAC with the 350 Disk File for $35,000 per year.

Although the size of the 350 Disk File—60×68×29 in.—bears little resemblance to modern disk drives, its electromechanical design is remarkably similar to that of today's drives. It used a stack of iron-oxide-coated aluminum platters with magnetic-recording surfaces on each side. But it used only a single pair of heads that a motor had to move to predetermined positions on a vertical "way" to the disk of interest. Once the heads reached the correct position, a pneumatic cylinder moved the heads laterally to a position straddling the platter of interest. Amazingly, the design achieved a maximum seek time of 0.7 sec, and an NRZ (non-return-to-zero) recording scheme yielded a transfer rate close to 9 kbytes/sec.

Perhaps the best technical account of RAMAC and the Disk File is from the MHDC (Magnetic Disk Heritage Center, www.sjmdhc.org). The MHDC hosts an exhibit in the building that housed the original IBM lab. The MDHC pegs several other milestones that came on the heels of RAMAC that refined the electromechanical design in today's disk drives. Even before IBM delivered RAMAC, the lab was working on the prototype of the ADF (Advanced Disk File), which would appear in 1961 in the 50-Mbyte IBM 1301. The ADF achieved what IBM called "real-time, online, direct-access storage" by dedicating a flying head to each surface. In contrast, IBM pitched the RAMAC Disk File as "online, direct-access storage." The ADF also pioneered perpendicular recording, although both RAMAC and products that appeared after the 1301 used longitudinal recording.

Later, IBM added servo-control information stored on the disks in the SDF (Single-Disk File); both RAMAC and ADF used open-loop control systems. SDF technology came to market as the IBM 3330 in 1971. The 3330 featured a 2-Mbyte removable disk pack, although the fixed-platter design returned later and remains the high-volume architecture. And the capacity march has never slowed. Today, for instance, Hitachi ships 1-in. Microdrives that store 8 Gbytes. Some projections have small MP3 players storing 3 Tbytes or more by 2020. EDN

11.01.56

Random Memory

Latest News Flashes

NEW YORK, N.Y.—Built around the IBM disc memory, a random access memory unit has a storage capacity of 5,000,000 digits. Any of these digits can be reached directly without scanning through intervening records. The memory unit consists of 50 magnetic metal discs arranged in a vertical stack. Both sides of the discs are used for recording data, so 100 disc faces are available for storage. There are 100 recording tracks on each disc face, and each track will hold a stack of ten 100-character records. The entire stack rotates at 1200 rpm, so that any address in the memory can be located in milliseconds.

The 50-platter IBM 350 Disk File featured a single pair of heads that moved vertically to reach the platter of interest and yielded a maximum seek time of 0.7 sec (courtesy Magnetic Disk Heritage Center).

Designed and produced by IBM, the Model 305 RAMAC uses punched card input and punched card and printer output. This data processing machine relies upon a powerful combination of stored program and control panel wiring for instructions.

***EDN*, November 1956**

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BY HOWARD JOHNSON, PhD

Terminator II

In my last column, I presented a rather troubled system architecture with incredibly stringent signal-quality requirements (**Reference 1**). The signal source is a low-impedance ECL driver with a 400-psec rise time, which connects to the receiver by 3 ft of RG58 A/U coaxial cable.

Somebody else already built the signal source, so you are stuck with the low-impedance ECL output. By government contract, you must design the receiver using an off-the-shelf FPGA combined with an external 50Ω±1% terminating resistor.

So far, the termination strategy sounds good, but unfortunately, the FPGA has a 9-pF input capacitance (**Figure 1**). When it connects directly to the external 50Ω end-terminating resistor with R_2=0Ω, the input capacitance interferes with the operation of the termination, creating massive reflections. The reflections return every 8 nsec, commensurate with the round-trip delay of the coaxial cable.

Quantifying the impedances in this circuit, the 400-psec rise time corresponds to a frequency of roughly F=0.35/(400 psec)=875 MHz. At that frequency, the 9-pF capacitance of the FPGA inputs presents an impedance magnitude ($1/(2\pi FC_{IN})$) of just 20Ω. This low impedance loads the 50Ω termination, preventing the terminator from doing its job.

Resistor R_2 acts as an isolation component, preventing the FPGA capacitance from directly loading the terminating resistor.

Now, insert resistor R_2 with a value of 50Ω in series with the FPGA input. This circuit trick raises the effective input impedance of the FPGA to something *at least* 50Ω or greater. In the worst-case scenario, if the capacitor impedance were absolutely zero, the parallel combination of R_1 and R_2 would make a termination impedance of 25Ω, creating a reflection coefficient no larger than one-third.

Resistor R_2 acts as an isolation component, preventing the FPGA capacitance from directly loading the terminating resistor. A value of 50Ω for R_2 in this circuit yields a fourfold reduction in the reflected signal amplitude.

At the same time, resistor R_2 degrades the received-signal rise time. This situation occurs because the combination of R_2 and C_{IN} acts as an RC lowpass filter. Setting R_2 equal to 50Ω in this circuit doubles the signal rise time.

If you are worried about late reflections shifting the apparent times of arrival for subsequent edges, the induced jitter varies in proportion to the product of the reflected signal amplitude (as a fraction of the signal swing) times the signal rise time. If the reflections decrease fourfold but the rise time doubles, then you win a twofold reduction in jitter. That outcome is good, but I want to do better.

In my next column, I will show you how to force the termination impedance to equal exactly 50Ω with minimum degradation of the received-signal rise time. EDN

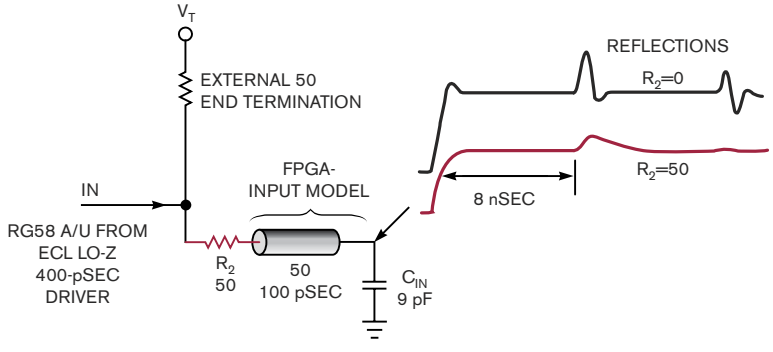

Figure 1 Adding 50Ω resistor R_2 raises the termination impedance, reducing reflections, but degrades the signal rise time.

REFERENCE

1 Johnson, Howard, "Terminator," *EDN*, March 2, 2006, pg 26, www.edn.com/article/CA6309116.

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Go to www.edn.com/060330hj and click on Feedback Loop to post a comment on this column.

Howard Johnson, PhD, of Signal Consulting, frequently conducts technical workshops for digital engineers at Oxford University and other sites worldwide. Visit his Web site at www.sigcon.com or e-mail him at howie03@sigcon.com.

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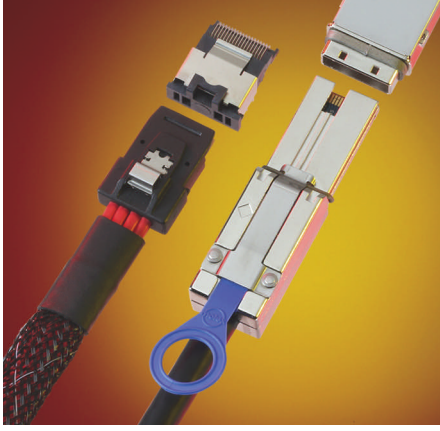

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BY JOSHUA ISRAELSOHN, CONTRIBUTING TECHNICAL EDITOR

Scaling: a balanced view, part one

I've long maintained that, as long as semiconductor vendors use process descriptors to promote IC products, OEM designers need to know enough about those processes' capabilities to distinguish reasonable claims from hype (**Reference 1**). Leaving aside fond memories of IC processes that can support ±15 and ±18V rails, analog-IC designers began more than a decade ago to feel the pinch of process-imposed voltage scaling when the minimum feature size slipped below 700 nm and forced supply rails to do what was theretofore unthinkable: fall below 5V.

Since that time, claims about process scaling have all too often come down to the oversimplification, "good for digital, bad for analog." Although one cannot argue that scaling has been good for digital designers, the claim that it is bad for analog design depends upon certain assumptions that do not always hold. Additionally, many discussions about submicron and deep-submicron analog processes observe the effect that scaling has on parametric performance, whereas, in practice, performance is rarely a negotiable consequence of process selection. Instead, the application determines the minimum acceptable performance. So, the notion that scaling a process necessarily results in a degradation of, say, SNR, gains little traction if, to be competitive, a product must meet or exceed a specific minimum performance with respect to that parameter.

I mention this fact because Klaas Bult of Broadcom Netherlands presented an insightful analysis on the effect of technology scaling on power dissipation in analog circuits at the ISSCC (International Solid State Circuits Conference) in February (**Reference 2**). The conference organizers have not yet widely distributed the work, so here begins a summary, which I will continue in the next installment of this column.

Bult observes that, within broad limits, "power can buy any performance"; as the *currency of the realm*, power dissipation thus appears in the denominator of a great many figures of merit. The key question, then, is: For a given level of performance, what effect does the voltage scaling have on power dissipation? The answer depends upon the performance parameters of interest. Using a single-transistor gain stage as the model minimum subcircuit, Bult observes, distortion, slew rate, settling, and bandwidth follow the bias current, whereas matching, white noise, and 1/f noise follow the load capacitance (**Figure 1**). The minimum subcircuit forms the basis of higher order subcircuits, such as differential pairs and gain cells with explicit feedback networks. From this scenario, Bult suggests an analysis that calculates the minimum dissipation that the subcircuit string requires to support a given level of performance with feature size as a parameter (**Figure 2**). Though the detailed analysis is not the sort of exercise OEM designers need to perform, an understanding of the concepts that the analysis draws upon can result in a clearer understanding of the implications that process scaling has on parameters of interest. The next installment of this column will continue with this thought. EDN

REFERENCES

1 Israelsohn, Joshua, "Ripples in the process pool," *EDN*, Jan 24, 2002, pg 44, www.edn.com/article/CA191157.
2 Bult, Klaas, "The effect of technology scaling on power dissipation in analog circuits," ISSCC 2006, Feb 5, 2006.

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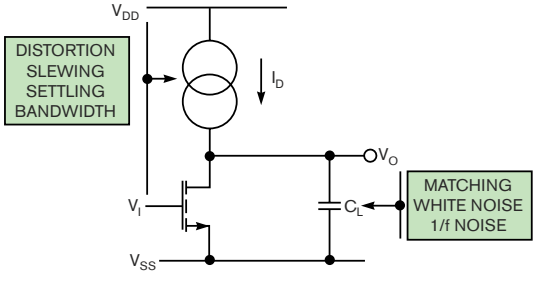

Figure 1 A single-transistor gain stage serves as Bult's model minimum subcircuit.

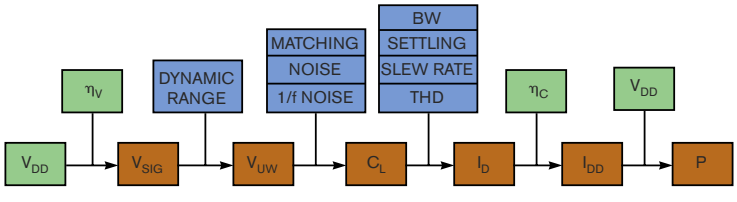

Figure 2 Bult's analysis combines application requirements (blue) with terms that derive from the process scale (green) to generate calculated values (brown) resulting in a power estimate for the model subcircuit.

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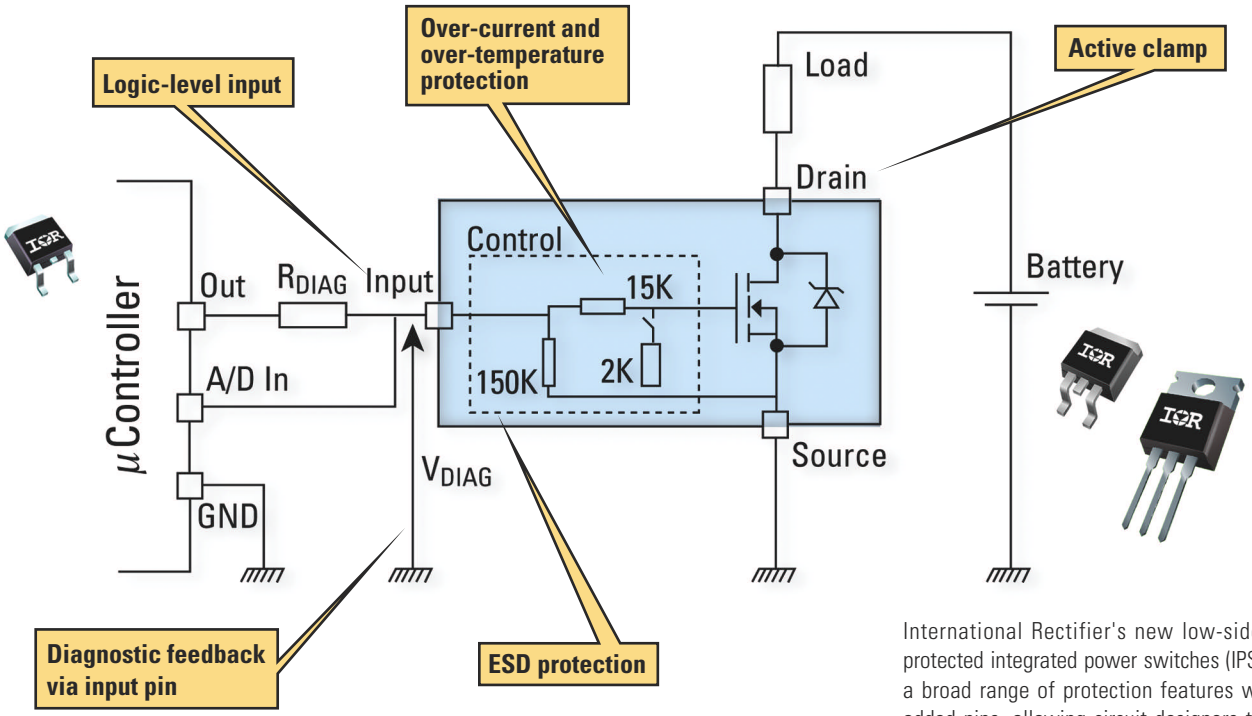

Part Number	Package	$R_{DS(on)}$ max. (mΩ)	V_{CLAMP} min. (V)	Over-Current Shutdown Typ. (A)	Quality Level
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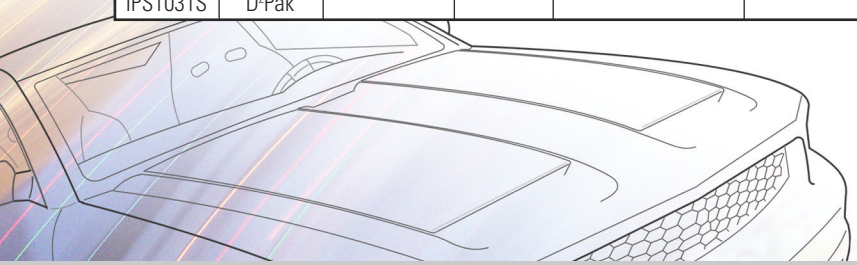
IPS1021 IPS1021R IPS1021S	TO-220 D-Pak D²Pak	25	36	45	Q100, MSL1
IPS1031 IPS1031R IPS1031S	TO-220 D-Pak D²Pak	50	36	18	Q100, MSL1



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Strange but true stories from the call logs of Analog Devices

Contributing Writer James Bryant has been a European Applications Manager with Analog Devices since 1982. He holds a degree in Physics and Philosophy from the University of Leeds. He is also C.Eng., Eur.Eng., MIEE, and an FBIS. In addition to his passion for engineering, James is a radio ham and holds the call sign G4CLF.

Grounding Converters (or philosophy to the rescue!)

Q. *I can't believe that you recently advised us to connect the digital ground pin of ADCs to the system analog ground. Was this a mistake?*

A. That was no mistake. It's the only safe way to connect data converters (ADCs and DACs) that have separate analog (AGND) and digital (DGND) ground connections. Your horror is the result of a philosophical error known as a "category mistake." Fortunately, I know something about philosophy as well as electronic engineering so let me explain.

A category mistake occurs when we assume that because two objects have the same, or similar, names then they are the same thing, or the same sort of thing. The name here is "digital ground." The digital ground is the part of the system ground that carries the ground currents of the system's digital circuitry. In a converter, the digital ground (DGND) is the pin that carries the supply current from the converter's digital circuitry and the return current from its digital interfaces.

These are not the same thing. The optimum connection of a converter's DGND pin is to its AGND pin, i.e., at the IC package and at exactly the same potential. This minimizes capacitive crosstalk between the two grounds in the chip and hence logic related noise in the converter output. Where possible, of course, it is better for a converter to have a single common internal analog and digital ground, but the voltage drop due to the digital ground current flowing in the pin impedance often makes this impossible, so separate AGND and DGND pins are essential.

But they must be joined at the package[1] and nowhere else. I have noted before that data sheets are often less than ideal — sometimes a converter data sheet may recommend that AGND and DGND are connected to system analog and digital grounds respectively. When a data sheet tells you to do this it is incorrect, and you should ignore it.[2]

Furthermore, it is rarely advisable to locate the star point of the system analog ground and the system digital ground at a data converter — it should be near the power supplies. If the ground impedances are as low as they should be, this arrangement will slightly lower the noise immunity of the converter's digital interfaces, which should not matter, but will greatly improve the noise performance of the analog part of the system, which matters a lot.

[1] And with the lowest possible impedance — do not separate them with resistors, inductors or ferrite beads.

[2] There is a single exception to this rule, which is discussed in the longer text accessed by the link.

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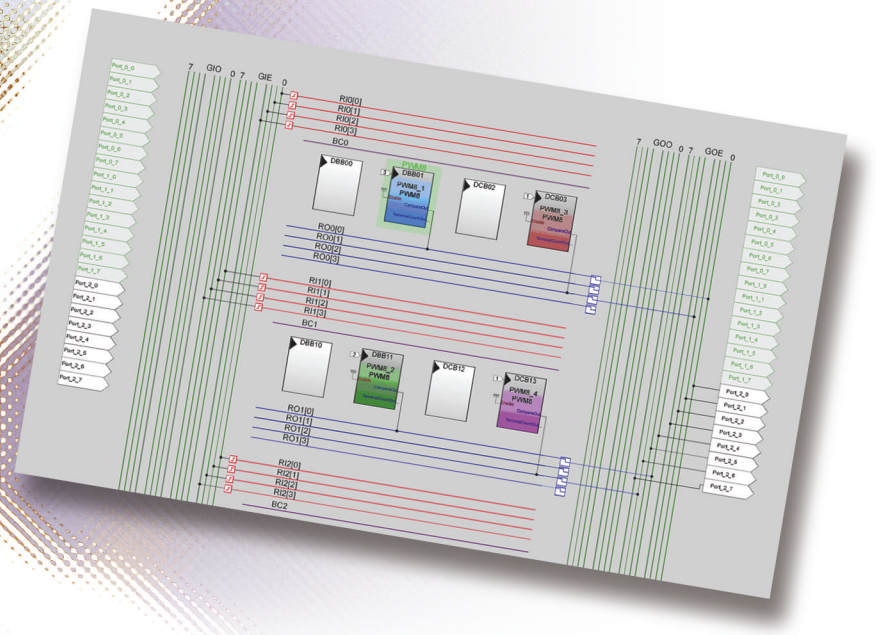

In this layout of the PSoC, the buses on the left serve as inputs to configuration blocks and connect to external pins by means of the traces above the blocks. The buses on the right connect to external pins as outputs using the traces below the configuration blocks. Note that every other block is empty in this view; these empty spaces are counter blocks that appear using a different view and have their own connections.

HANDS-ON PROJECT:

designing microcontrollers with low-cost reconfigurability

RECONFIGURABLE MICROCONTROLLERS OFFER AN IMPRESSIVE ARRAY OF ANALOG AND DIGITAL FEATURES TO MEET YOUR APPLICATION'S REQUIREMENTS.

Microcontrollers are often complete SOCs (systems on chips). Connect power and ground to a programmed device, and you have a powerful processor with active and ready memory and peripherals. These features drastically reduce design time, because using microcontrollers effectively eliminates the job of integrating components and peripherals.

Many of today's 8-bit microcontrollers offer an impressive combination of integrated features and interfaces, including hardware-based ADCs and DACs, PWM support, and a range of serial and parallel interfaces. For small systems, a microcontroller often provides all of the peripherals and interfaces an application requires. The primary limitation of these devices, however, is the quantity and quality of the interfaces. For example, a microcontroller might support a 12-bit ADC on only two of 13 interface pins. If you need three ADCs or one with 14 bits, you must take a different approach.

This hands-on project focuses on cost-effective flexibility for designing a general-purpose sensing and control module as the foundation for a range of applications. Requirements for the microprocessor included the ability to operate simple user-interface devices, such as LEDs, buttons, dials, and LCDs; to accept data from sensors having a range of data bits and sampling frequencies; and to control analog and digital peripherals, including motors and analog-output devices. The design had to support data logging to a centralized location, including both data-collection and -transport mechanisms. It also had to support mesh and hierarchical networks, allowing the ability to tier multiple modules through hub, daisy-chain, or peer-to-peer architectures.

GAINING FLEXIBILITY

Unfortunately, 8-bit microcontrollers support a limited array of interfaces, and I wanted to be able to support a wide range of applications requiring a varied number of PWMs, ADCs, DACs, and serial interfaces. In my search for a flexible microcontroller, I found the PSoC (programmable-system-on-chip) family from Cypress Semiconductor (www.cypress.com), which employs reconfigurable-logic gates and a switching fabric to define interface-pin functions. PSoC devices cost a little more than microcontrollers of the same functional magnitude, depending on your application.

AT A GLANCE

- Reconfigurable microcontrollers can provide hardware-based processing without the complexity of synthesis.
- Through reconfigurability, microcontrollers can overcome interface-allocation limitations typical of fixed-configuration microcontrollers.
- Reconfigurable microcontrollers enable a higher degree of flexibility for applications requiring a wide range of I/O options, such as aggregators and expanders.
- Reconfigurable architectures have their limitations, but focusing on their abilities enables engineers to cost-effectively extend functions over time.

I was initially wary of looking at a PSoC. I wanted flexible reconfigurability but not at the expense of having to learn a VHDL and synthesis environment to create simple interfaces to LEDs, sensors, and motors. PSoCs, however, avoid this added design complexity. Developers cannot individually access the logic gates within the PSoC; they must instead access them from a functional level. As long as enough resources are available to implement a block, they can define complex combinations of functions and route them to various interface pins.

Designers implement digital and analog functions using configurable blocks. Some blocks perform analog functions, and some perform digital functions. These functions connect through a fabric that eliminates the need to route power, ground, and signal lines among multiple ICs. By allocating additional resource blocks, you can implement complex signal conditioning in hardware, providing high performance without consuming precious processor cycles. You can combine a variety of blocks to create a one-chip mixed-signal design. In the PSoC-development environment, you can select preset functional blocks, such as an 8-bit PWM or a 16-bit ADC, that you want to implement. You can initialize these locked blocks at power-up through registers in flash memory and dynamically reconfigure them through software APIs (application-programming interfaces), but the PSoC predefines the blocks' basic functions.

This limited configurability, however, is one of the PSoC's greatest strengths. Because the blocks are predefined, I brought up a working PWM in minutes without delving into logic schematics or deciphering preconfigured code. With a bit more work, I was able to quickly and repeatedly replicate the PWM. Given the simplicity of a defined block, all of the API code is consistent and straightforward to use.

MANAGING CONFIGURATION

I did encounter some difficulties in using multiple copies of the same functional block. I employed a naming convention of PWMx, hoping to make extensive use of macros and subroutines. I found it challenging to reorder and reroute blocks once I had placed them, however. I had placed PWM3 between PWM1 and PWM2 and wanted to rectify this misordering. I had to delete both PWM3 and PWM2 and then redefine them in the proper position to accomplish this task, which I couldn't do easily using drag-and-drop functions. Perhaps, if I had more experience with the tools, I might have been able to do so. However, simultaneously designing hardware and software is a new approach for me, and I had not yet discovered all the tricks and strategies that separate the experts from the novices.

THIS PROJECT WOULD HAVE NEEDED A COMPLETE REDESIGN TO MINIMIZE LATENCY AND THE AMOUNT OF TIME THE PWM HELD UP THE MICROCONTROLLER PROCESSOR.

From this lesson, I learned that you must carefully allocate analog and digital resources and interface pins. Early, haphazard placement of blocks can isolate resources in such a way that you may be unable to assemble them to form a more complex function, or you may lock out the use of certain output pins. For example, I had enough resources to implement an I^2C interface but not where I needed to—that is, using specific I/O pins because of how I had previously allocated other blocks and functions. Reallocating resources, a rather tedious process, solved this problem, which I could have avoided through planning placement rather than immediately allocating resources.

Another problem I encountered was that the compiler does not support macros within macros, which makes it difficult to create multiple copies of individual blocks of code for each instantiation of a function. For example, a generalized PWM macro cannot call a second specialized macro, significantly reducing the utility of macros. Alternatively, PSoCs support an indirect referencing mechanism that you can use to emulate a record structure for easily passing groups of associated variables and offsets into function vectors. This approach saves program memory but can increase latency because it makes the function indirect and abstract.

The indirect-referencing mechanism, however, took me some work to figure out. The development kit includes a sparse handful of application examples. The memory-allocation model for the compiler has several variations, and none of the applications provide an example of how to successfully declare a variable. Additionally, once I did figure out how to declare variables, I had trouble directly and indirectly referencing them. I partially blame myself for these early difficulties, but the primary cause is the documentation that comes with the PSoC-development environment. The electronic manuals provide little help and no examples of how to declare variables within the memory models. The pseudocode doesn't work unless you correctly place it within the framework, and the manual contains no reference on how to do so. Fortunately, I discovered a resource outlining ways to avoid many of these headaches that saved me from making time-consuming mistakes (**Reference 1**).

Admittedly, many of these difficulties are mere annoyances rather than fatal flaws. Most vendor-based tools lack adequate documentation. Cypress, for its

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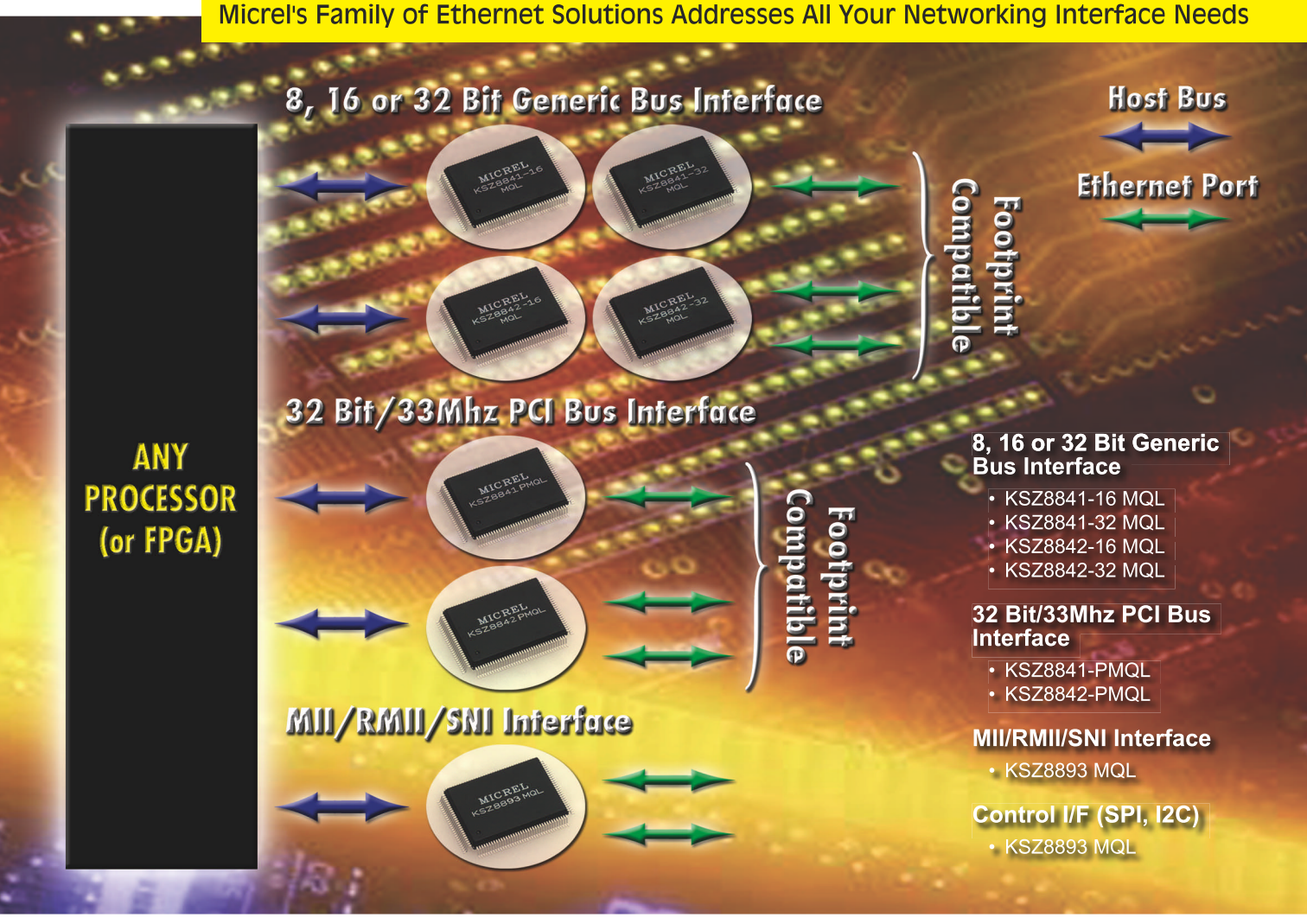

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part, has a history of addressing the more problematic limitations in updates.

LIMITED CONFIGURABILITY

Limited configurability is a key element of quickly getting up to speed on a PSoC. The other side of limited configurability, however, is that, once you know what you're doing, you can't modify the hardware blocks. For example, I created several regularly used functions, including ramp-up and -down using the PWM to provide a smooth drop-off. This straightforward function effectively reduces the duty cycle of the PWM. I used a hardware timer and interrupt to implement this function, which consumed many processor cycles and introduced a burst of interrupts.

However, when several PWMs are simultaneously ramping, the load on the processor greatly affects the rest of the application. Additionally, having so many simultaneous interrupts to manage can break an application's real-time determinism. My application had no real-time latency constraints, so I was able to ignore the interrupt contention but still had to struggle with loading on the processor. Alternatively, I considered tying the ramping function of multiple PWMs to a single interrupt to reduce the number of interrupts, but this approach would have impaired my ability to isolate each PWM from an object perspective.

Ideally, I would have liked the ability to implement the ramping function within the configurable fabric, but PSoC doesn't allow you to modify configurable blocks. The function is simple enough and provides the benefit of offloading the processor. Altering hardware-function blocks would have enabled me to further protect my design; burying some intellectual property in the hardware partition makes it more difficult to reverse-engineer a design. This feature is especially relevant if a design must support field upgrades; even if a processor offers hardware-code protection, the code becomes exposed even when it is available only as a binary file. The reality is that the hardware blocks are equivalent to library files for which you lack the source code, which enables you to define and successfully use programmable gates without knowing what is happening inside the chip.

SOFTWARE CONTENTION

One advantage of working with a programmable mixed-signal part is that a straightforward partitioning of real-time and application code exists between hardware and software. Even with a fixed-implementation microcontroller, for example, it is relatively simple to implement a PWM. One PWM requires only one timer and integrates well with other system events. Scaling a design, however, is a different matter from implementing a single instance. Using a component method, you can hammer out the details, in this case, of a single PWM. However, the requirement for several simultaneously operating PWMs can be beyond the ability of a traditional microcontroller.

A microcontroller might offer several PWMs, for example, but any application that requires more than the offered number meets a barrier. The next PWM brings with it the cost of implementing it in software. This extra work introduces resistance to entering new markets that require only a nominal incremental increase in capabilities. Adding a second extra PWM is not simply a matter of duplicating the first software PWM. When you implement a PWM in hardware, it has no effect—other than during dynamic reconfiguration—on the main processor. Implementing several PWMs in software raises significant interrupt-scheduling, contention, and real-time-processing issues, because the approach stretches, for example, timer resources to their limits. Furthermore, interrupt handling consumes overhead and introduces synchronization issues—that is, several interrupts can occur simultaneously and require immediate servicing. Also, application code now must compete with high-priority real-time-event processing.

At this point, this project would have needed a complete redesign to minimize latency and the amount of time the PWM held up the microcontroller processor. This design effort is not trivial; furthermore, it focuses on enabling rather than creating an implementation. In other words, I would not be creating any new value, per se, but rather trying to cram working functions into the available space. If the project had used a software PWM from a library, then I might have also had to break into this code to resolve contention issues.

Contention is a serious design consideration that increases disproportionately when you scale a design. As resource sharing within a design increases, so does the

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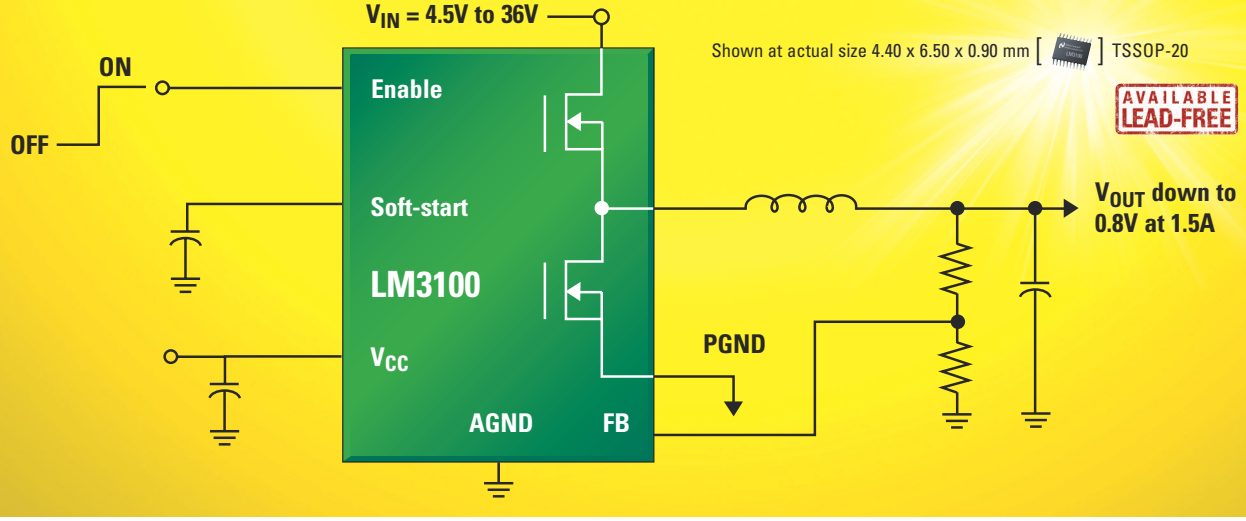

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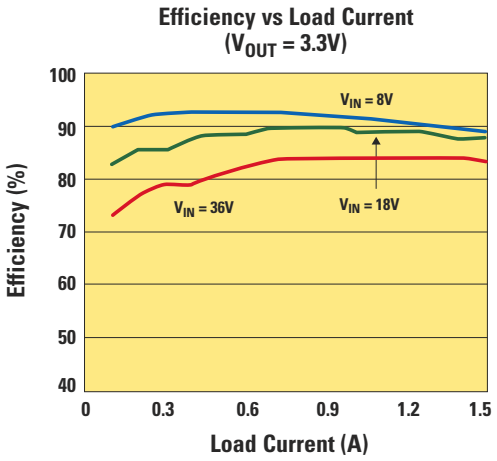

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percentage of design effort that you need to focus on simply resolving contention. Even using the PSoC involves issues of managing all of the dynamic changes that require reconfiguration of the PWMs and management of the other functional blocks. An even larger drain on processor and application resources would occur if the design also had to share CPU cycles with the basic PWM function itself.

MODULE CONSIDERATIONS

This project could have used one of several architectural approaches for the sensing and control module. For example, a module can be either external or a direct implementation on the pc board. I could choose to route I/O interfaces using either switches or generic connectors. Given the integration level of PSoCs, I might even have considered using the chip itself as the entire module; at one point, I reduced a version of my design to a single PSoC and voltage regulator on a breadboard.

Alternatively, I could have created an external module to expand the available I/O interfaces. For example, I worked with the idea of connecting my module to the main system through an I^2C bus. The module operates as a stand-alone subsystem responsible for all of the I/O that connects to it. The main system has access and control over this I/O through a proprietary protocol that passes over the I^2C bus.

In the end, the question boils down to just how much flexibility you can take advantage of. Because of the relatively low initial production run of my design, reducing the number of overall designs offers substantial cost savings. For example, I could build a sensing system using a range of components with modules for a number of high-volume configurations and one module to handle all the other configurations. However, each of these optimized modules would require its own NRE (nonrecurring-engineering) charges. At some point, the time and engineering costs to implement several such components becomes excessive, and the implementation would also exceed the available time. In other words, can you spare the 50 hours it takes to shave 50 cents off of a configuration?

This trade-off is a complicated one to consider and depends upon how much time and money you have allocated to increasing product diversity and market share. The advantage of creating a flexible module is that it initially reduces NRE investment and inventory diversity. Additionally, it reduces the number of interactions with the factory and aggregates overall product volume, leading to a lower overall cost for the initial module. Also, at this stage in a design, you cannot predict which configurations will be high-volume sellers. You can later optimize a module for a configuration if the volumes for it prove adequate. You also don't have to deal with unsold inventory as the market matures; you can repurpose flexible components to sell at the full cost of the applications they can address rather than sell them at a deep discount.

Evaluating the trade-off between potential cost savings of optimizing an architecture for high volumes and maintaining a single base architecture across multiple applications is important. Modules, by their nature, segment functions between software and hardware components. This segmentation can complicate later optimization because modules act independently of other system components. For example, the module for this project had to be a complete and independent system. Therefore, the module must provide enough resources to create a smart sensing system that can capture, evaluate, and transmit data. However, if the sensors for an application require little processing, these resources will sit idle because they are so difficult to make accessible to other system components.

For my project, the fact that I chose to implement 16 interfaces introduced cost inefficiencies. Consider an application that requires 39 I/O interfaces. A 16-interface module can provide 15 interfaces: A minimum of one interface—two for some buses—links the module to other modules, and modules acting as hubs require $n-1$ interfaces. Three modules have 48 interfaces, four of which connect two modules to the third, which acts as a hub. This scenario leaves five unused interfaces. Additionally, an integrated approach would eliminate the need for the four communications interfaces. As a result, the device might have to bear the cost of as many as nine more interfaces than the application requires.

Another key source of both increased cost and increased unreliability is the need for a generic connector. The use of a generic connector extends the flexibility of a module. If I could guarantee that any application using a module would require a minimum number of LEDs,

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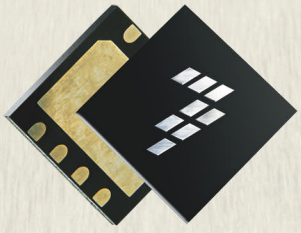

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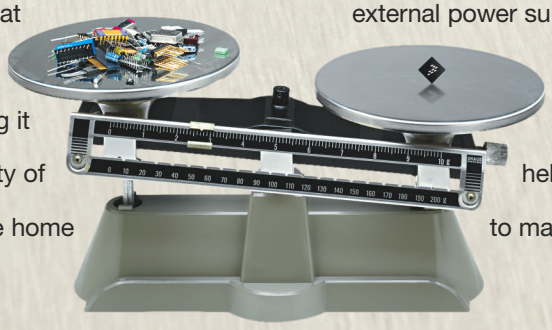

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motors, or I²C ports, I could have dedicated the appropriate number of interfaces and connectors. However, in many cases, the ability to cluster components on a single module lets you increase the intelligent processing on the module itself. For example, consider a system that requires 14 sensors and 14 LEDs. For one application, the LEDs display the status of each sensor. An LED that is continuously on means that the sensor is active, a flashing LED means that the sensor is experiencing an event, and an LED that is rapidly flashing means that the sensor needs servicing. For this application, it makes the most sense to group each LED with the appropriate sensor—seven sensors and seven LEDs per module with two I/Os reserved for a communications link.

On the other hand, the LEDs may convey information about the overall system based on aggregated processing of multiple sensors. For example, a group of sensors might monitor the same system component from different locations. Determining the status of the component requires using data from all of the sensors. If the group of sensors resides on two modules, then the modules may need to exchange a significant amount of data—introducing unwanted latency, as well—to resolve the status of the component. For this application, grouping the 14 sensors provides the most efficient means of intelligently managing the sensors. The sensor module would need to transfer only the state of each LED to the LED module. From a logical point of view, the LED module serves as an I/O expander for the sensor module, which itself is an I/O expander for the main system.

If the module configuration has constraints, such as a minimum or maximum available number of ADCs and LED drivers, more modules are necessary to provide the proper number of appropriate interfaces. Most traditional microcontrollers employ this architectural model. Although each microcontroller-product family offers a variety of interface configurations, these configurations have limited scope and scale. Given software-implementation limitations, it might require more microcontrollers than reconfigurable devices to implement a configuration.

With the availability of low-cost reconfigurable or field-programmable devices, designers of embedded-system applications, such as industrial-control, motor, LED, and sensor-management systems, can now implement functions in hardware rather than software, enabling developers to both consolidate system management in fewer processors and increase device flexibility through easily and dynamically adjusting hardware interfaces.

The primary trade-off occurs when you decide how much flexibility and what range of functions you need. This decision determines how closely a fixed-microcontroller architecture matches your application. For applications requiring two ADCs and a lot of general-purpose I/O, for example, an off-the-shelf microcontroller offers you a more integrated and less complex foundation. When the I/O of a design may change over time or an application needs more instances of a set function, such as a PWM, than microcontrollers typically offer, then a reconfigurable architecture offers a clear advantage.

Some engineers are pessimists. They look at a project and note all the ways they cannot use it. I tend to be optimistic. I understand that every product has its limitations, but what matters most about each product is what new innovations it enables me to create. A PSoC as a reconfigurable architecture offers many features that are beyond the scope of this project. However, it is exciting that PSoCs offer the flexibility of substantially extending my design simply by cracking into a new set of modules. EDN

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REFERENCE

1 Ashby, Robert, *Designer's Guide to the Cypress PSoC*, Newnes Publishing, 2005.

AUTHOR BIOGRAPHY

Nicholas Cravotta is a contributing technical editor for EDN. *When he isn't designing electronics or writing, he enjoys building kaleidoscopes and developing board and card games. You can reach him at editor@nicholascravotta.com.*

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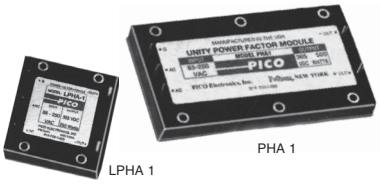

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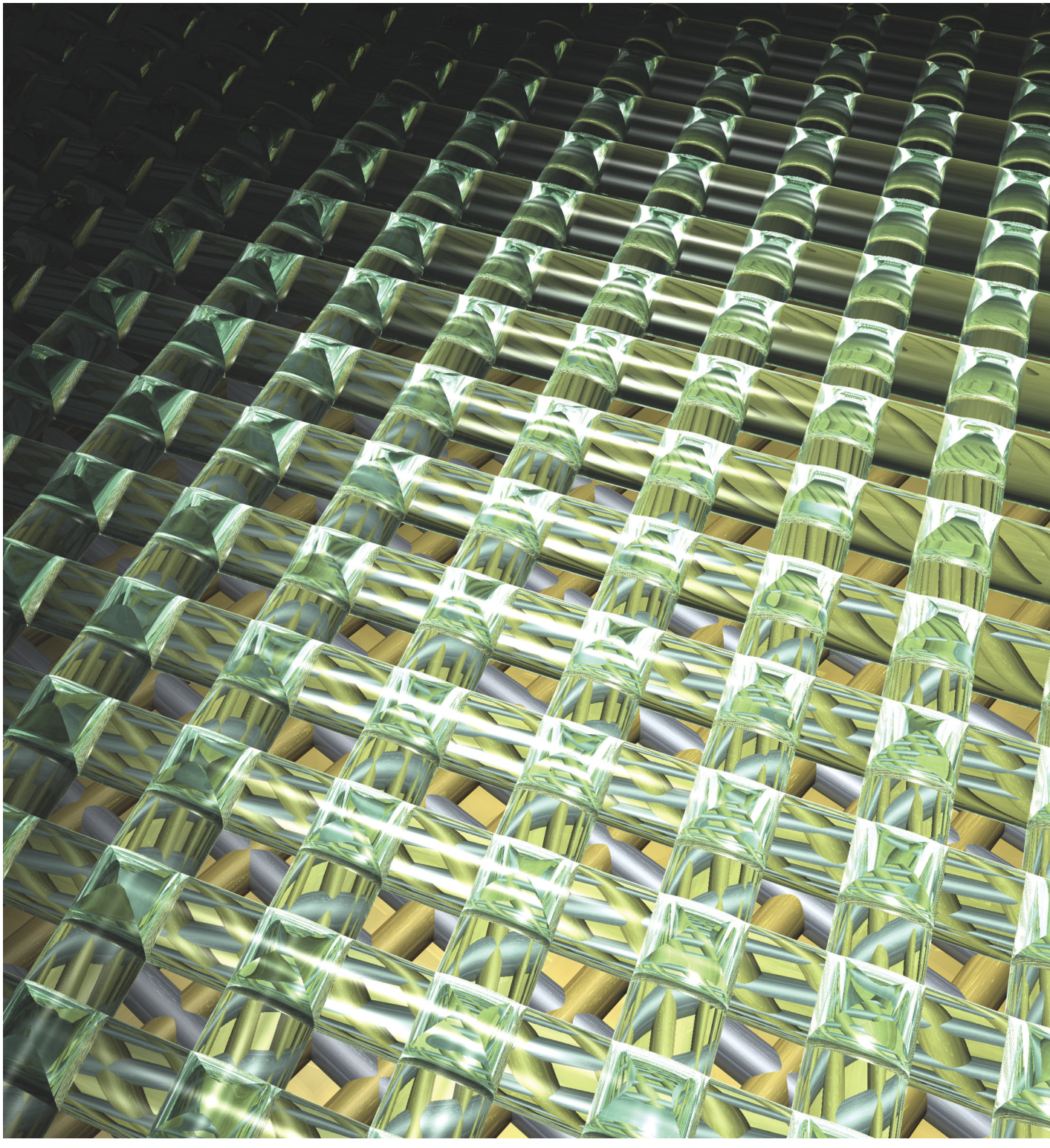
EPIC updates stretch

TWO NEW BOARD-LEVEL STANDARDS OFFER PC/104 DESIGNERS MORE REAL ESTATE, A LINK TO FABRIC TECHNOLOGY, AND CONTINUED COMPATIBILITY WITH LEGACY HARDWARE.



stackable systems

Since its introduction in 1992, PC/104 has been one of the most popular embedded-system architectures, because of its size, rugged construction, and PC compatibility, and due to the huge array of off-the-shelf components available to developers. Often embedded in medical instruments, avionics, vending machines, test equipment, communications devices, vehicular systems, data logging, and industrial-control systems, PC/104 products take advantage of the low-cost silicon, software, and development tools from the desktop world. Like all other long-term board standards, PC/104 has undergone several revisions to keep up with changes in technology. The latest additions, EPIC (Embedded Platform for Industrial Computing) and EPIC Express offer PC/104 designers a more flexible form factor and future access to high-bandwidth serial interconnections.

The developers of the PC/104 architecture based it on the ISA (Industry Standard Bus) from the IBM PC. The developers derived the name from the PC and the number of interface pins on the 16-bit ISA bus. Although the ISA bus is now essentially obsolete on the desktop, it still has advantages for embedded systems. Peripheral cards are simple, low-cost, and easy-to-design—all prime requirements of embedded products. The relatively low speed of the ISA bus also simplifies noise- and EMI-protection schemes. Yet, the main reason for its continued popularity is the large number of off-the-shelf products from which designers may choose. Currently, there are dozens of manufacturers actively producing hundreds of unique PC/104 products.

PC/104 cards have stack-through connectors that eliminate the need for a motherboard, backplane, or card cage. These pin-and-socket bus connectors provide a reliable signal path even in harsh environments. Although the stack-through connectors are among the positive features of PC/104, they also cause problems. Along with manufacturing headaches that connectors on both sides of the board cause, the densely packed PC/104 configuration makes it difficult to change boards, especially in the center of a stack. The PC/104 Consortium published a formal specification in 1992 that it maintains on its Web site.

COTS STACKABLES

Standard PC/104 modules come in a variety of simple and sophisticated configurations. For example, for mobile telematics, fleet management, distributed communication systems, and remote data-logging applications, the

AT A GLANCE

- PC/104 maintains its popularity because it gives embedded-system designers access to hundreds of off-the-shelf peripheral cards from multiple vendors.
- The ruggedized configuration and low size, weight, power, and cost of PC/104 modules make PC/104 an effective embedded-development platform.
- A new midsized baseboard specification gives designers enough real estate for a CPU and basic I/O and also preserves backward compatibility.
- The proposed EPIC (Embedded Platform for Industrial Computing) Express standard extends the PC/104 architecture with optional high-bandwidth PCI Express switched-fabric technology.

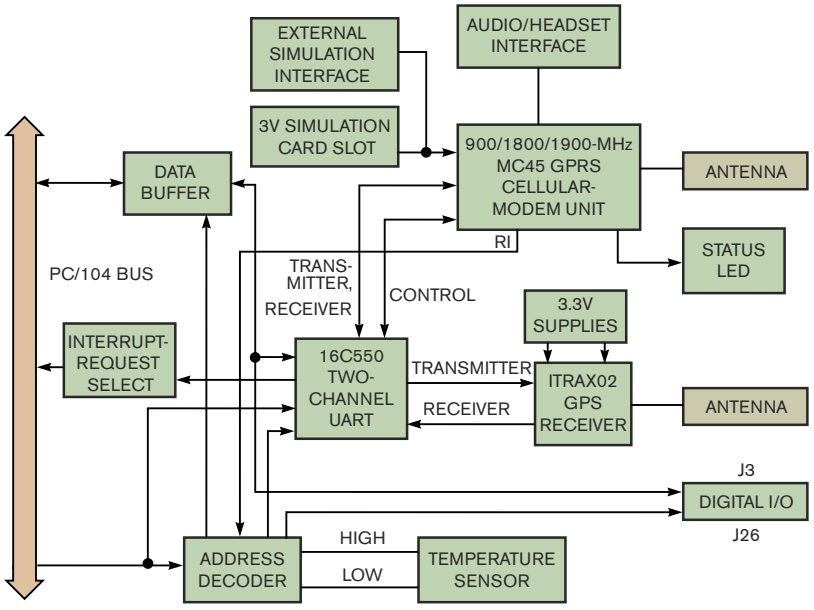


Figure 1 The Com17035er from RTD Embedded Technologies integrates a wireless modem unit and a low-power GPS receiver on a single PC/104 module.

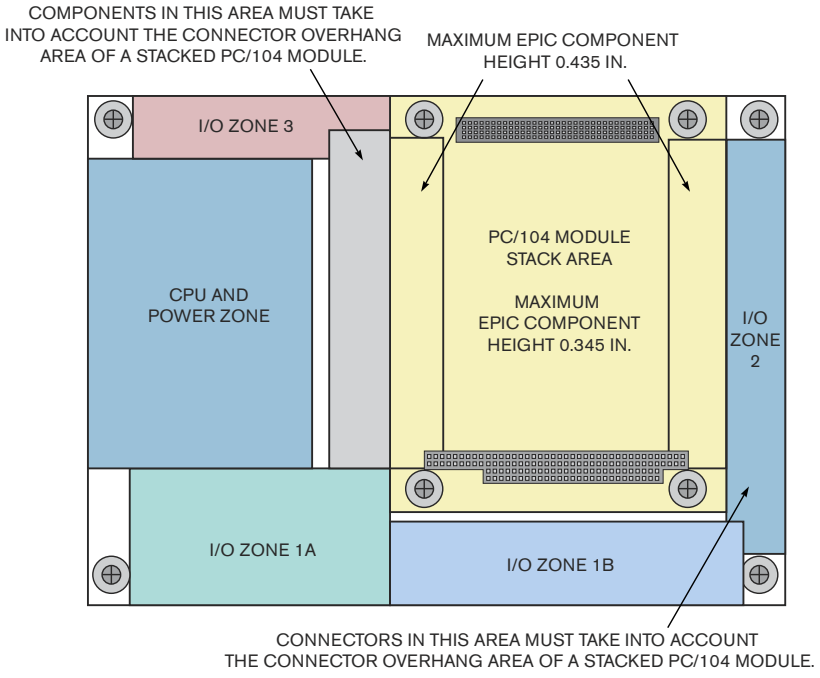


Figure 2 The EPIC specification defines a 4.5×6.5-in. board area with five board zones to accommodate large heat sinks and variable-height I/O connectors.

Com17035er from RTD Embedded Technologies combines a wireless dual-band modem unit and a low-power parallel-tracking GPS (global-positioning-system) receiver on a single PC/104 module (**Figure 1**). This module provides a direct connection to stationary or mobile GSM (Global System for Mobile communication) fields using the Siemens MC35 cellular engine in the 900-, 1800-, or 1900-MHz band. You can connect any standard GSM or GPS antenna directly to the Com17035er using onboard connectors. Key features include a maximum 50-kbps data rate, an onboard SIM-card socket, a headset interface, UART interfaces to a host computer, and a −20 to +70°C operating-temperature range. The module is compatible with all x86 operating systems, including DOS, Windows, Linux, and real-time operating systems, such as QNX, VxWorks, and Windows CE. Prices for the Com17035er module with adapter cable and antenna start at $695.

Since PC/104's introduction, designers have incorporated into it several enhancements to extend performance. The PCI bus has effectively replaced ISA on the desktop, and it was only natural for system architects to add it to PC/104. The PCI bus brings a much higher data rate for high-performance peripherals and application-specific hardware. The PC/104 Consortium in 1997 released the specification for the PCI extension, PC/104-Plus. It gives board designers the choice of incorporating the ISA bus

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alone, the PCI and ISA buses together, or the PCI bus alone. PC/104-Plus requires a new connector to house the PCI-bus pins, a loss of board space that is one of the few disadvantages of the PCI upgrade.

PC/104 got another boost in efficiency in 1997, when Ampro Computers and Motorola jointly developed the specification for the larger EBX (Embedded Board Expandable)-form-factor computer board. EBX boards measure 5.75×8-in. and are large enough to implement a full 32-bit system with CPU, memory, display interface, and basic I/O on a single board. EBX also has an integral PC/104-Plus expansion interface, so users can stack off-the-shelf peripherals boards to complete

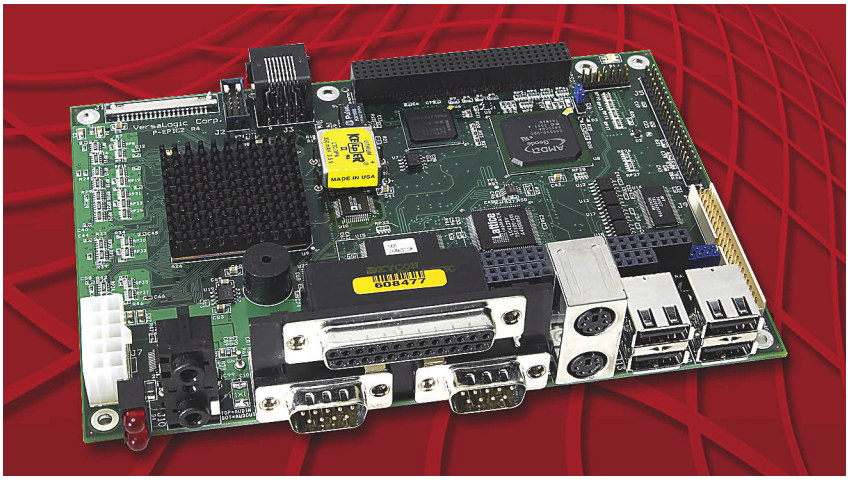


Figure 3 Operating from −40 to +85°C, VersaLogic's EPIC-format single-board computer delivers 500-MHz performance and draws only 1.5W.

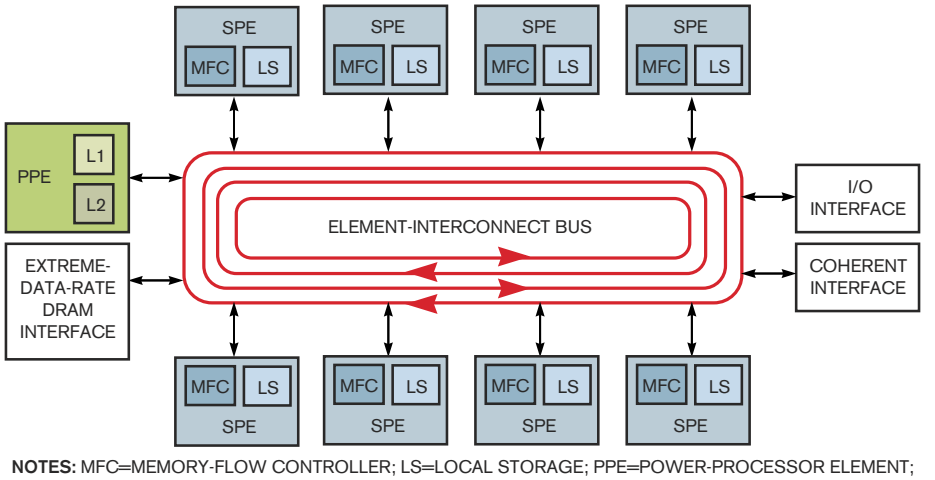
COMING DOWN THE PIKE

The ROHS (reduction-of-hazardous-substances) initiatives, cell-computing technology, and the multitude of fabric options were the hot topics at the January 2006 Bus&Board Conference in Long Beach, CA, sponsored by members of VITA (VMEbus International Trade Association). Although ROHS may have its biggest impact on manufacturing companies and fabrics are still battling for first place, cell computing may significantly impact the future of board design.

Eran Strod, director of product marketing at Mercury Computer Systems, summarized the cell architecture, which Sony, IBM, and Toshiba developed: "The cell broadband engine processor is the most significant architectural advance in high-performance embedded computing since vendors introduced AltiVec-enabled processors more than a decade ago. Originally driven by the needs of the entertainment and gaming industries, the cell processor is the result of collaboration among the companies.

"The architecture of the cell processor features nine microprocessors on one chip: eight SPEs [synergistic processor elements] and a power architecture-compliant core, the PPE [power-processor element], which orchestrates their activities [Figure A]. The EIB [element-interconnect bus] provides the internal communication among the processors, moving 96 bytes/cycle. A DRAM controller provides memory access as fast as 24 Gbytes/sec. This new architecture is essentially a multicomputer on a chip.

"The processor delivers 200 Gflops for 32-bit floating-point operations, an order of magnitude beyond any previous microprocessor. When mapping real applications onto the cell processor, Mercury Computer Systems achieved performance improvements of five to 100 times that of currently available processors and estimated performance-per-watt improvements ranging from three to 10 times that of other available solutions."



NOTES: MFC=MEMORY-FLOW CONTROLLER; LS=LOCAL STORAGE; PPE=POWER-PROCESSOR ELEMENT; AND SPE=SYNERGISTIC-PROCESSING ELEMENT.

Figure A Basically a multicomputer on a chip for gaming, the cell broadband engine features nine microprocessors on a single chip.

14-Bit, 190 MSPS ADC

Speed and Performance

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ADS5444	13 Bits	250 MSPS	68.6 dBFS at 230 MHz IF	78 dBc at 230 MHz IF
ADS5440	13 Bits	210 MSPS	69.1 dBFS at 230 MHz IF	79 dBc at 230 MHz IF

The new high-performance, low-power ADS5546 ADC from Texas Instruments features 1.1W total power consumption in an ultra-small, 7mm x 7mm QFN package. It supports both high SNR and SFDR at high input frequencies and offers unprecedented interface flexibility with user-selectable CMOS or DDR LVDS outputs. The ADS5546 is ideal for demanding applications such as wireless communications, video, imaging, instrumentation, test and measurement.

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a system. The EBX specification does little more than state the board's mechanical dimensions, leaving the designer free to implement almost any computer configuration.

ENTER EPIC

To address the board-space problem and retain a more compact configuration, Micro/sys, Octagon Systems, VersaLogic, WinSystems, and Ampro Computers joined forces to create EPIC—a new, midsized, open-architecture, embedded platform. This board is large enough for the latest CPU silicon along with basic I/O, and it maintains compatibility with PC/104 and PC/104-Plus expansion modules. The new EPIC module has a 4.5×6.5-in. footprint, a little more than twice the area of a standard PC/104 board. The EPIC specification, also available from the PC/104 Consortium, defines five board zones to accommodate large heat sinks and variable-height I/O connectors (**Figure 2**). Although the specification does not address functions or connectors, these zones preserve component-height limitations, connector spacing, and mounting-hole locations.

With potential application in medical devices, security equipment, industrial machinery, aerospace projects, and transportation systems, VersaLogic's latest EPIC-format single-board computer, the Gecko, operates at −40 to +85°C (**Figure 3**). The company bases the Gecko on the AMD GX-500 processor, which offers 500-MHz-equivalent performance and draws only about 1.5W. The low power consumption results in minimal heat dissipation, eliminating the need for an onboard fan. The module's features include maximum 512-Mbyte DDR RAM, integrated video with analog and LVDS (low-voltage-differential-signaling) flat-panel outputs, stereo-line in/out, 10/100 Ethernet, analog and digital I/O, four USB ports, four communication ports, LPT (line-printer-terminal) and IDE interfaces, and a CompactFlash socket. The PC/104-Plus site accommodates both PC/104 and PC/104-Plus modules for system expansion. The Gecko includes safety features such as transient-voltage-suppression devices for electrostatic-discharge protection, self-resetting fuses for user I/O, and a watchdog timer for hardware-level application control. Prices start at $673 (OEM quantities).

Targeting machine-to-machine applications, such as robotics, pipelines, medical, transportation, test equipment, security, machine control, HVAC systems that require a processor, a wide variety of I/O, and network connectivity, WinSystems recently introduced the EPX-GX (**Figure 4**). With 11 onboard I/O functions plus more I/O-expansion options through PC/104 modules, the EPIC-based module features the AMD GX500 processor, a Pentium-class CPU with an x86-native instruction set, and 32 kbytes

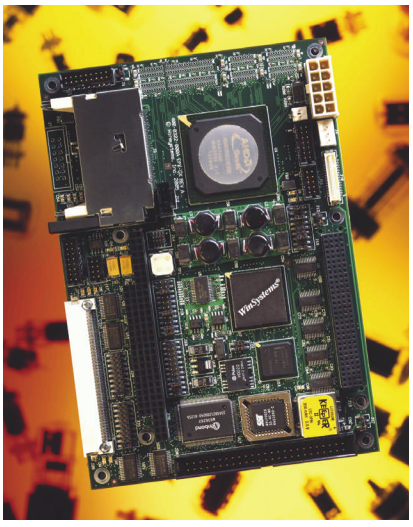


Figure 4 Featuring the AMD GX500 processor with integrated L1 cache, the EPX-GX from WinSystems offers a wide variety of I/O and network connectivity.

of integrated L1 cache that runs Windows CE, WindowsXP embedded, Linux, VxWorks, and QNX. Onboard I/O support includes 10/100 Ethernet, an 802.11 miniPCI connector, two USB ports, four communication ports, 24 parallel digital-I/O lines, 4× AGP video with a CRT and digital flat-panel interface, a keyboard controller, PS/2 mouse support, an LPT port, and AC'97 audio. The low-power design allows the EPX-GX to operate over the industrial-temperature range of −40 to +85°C without a fan. The EPX-GX draws typically 1.8A at 5V during normal operation. Delivery is stock to three weeks, and the price is $499 (OEM).

For expanded I/O applications, the new Micro/sys Opto104 accommodates eight industry-standard digital or analog Opto plug-in modules plus any PC/104 CPU or I/O cards you need to make a rugged, compact industrial controller. You can plug any combination of digital- or analog-I/O modules into this EPIC-sized board, which targets rugged environments and extended-temperature ranges of −40 to +85°C (**Figure 5**). Additional system-level features of the Opto104 include a watchdog timer; a rotary-encoder input; an onboard temperature sensor; and interfaces for a character-based LCD, keypad, and CAN (controller-area-network) bus. When applications demand additional I/O, you can connect as many as four Opto104 boards together in a slave configuration using a 26-wire ribbon cable. Opto104

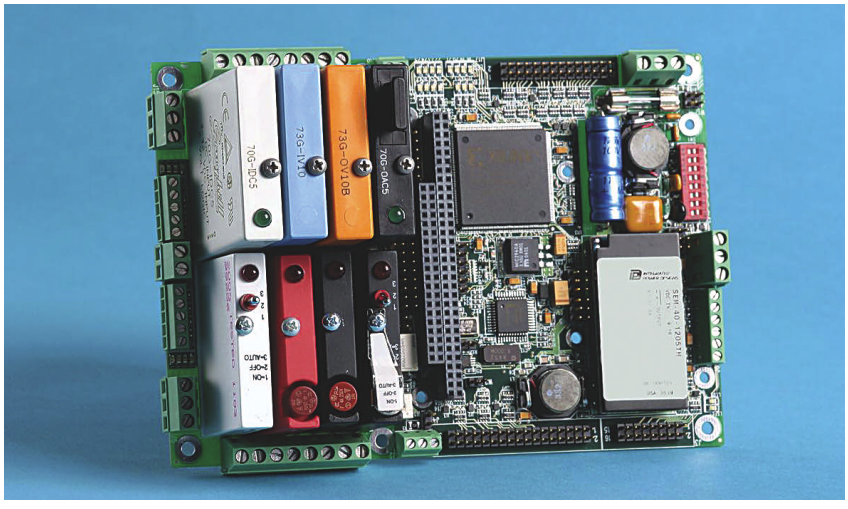
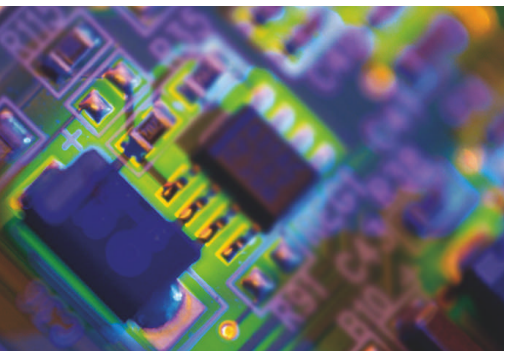
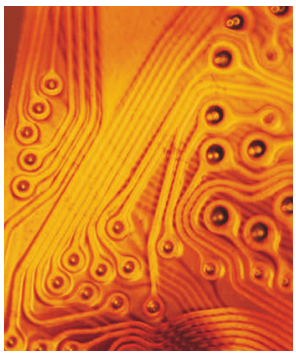


Figure 5 Micro/sys' Opto104 accommodates eight digital or analog plug-in modules plus PC/104 CPU or I/O cards to make a compact industrial controller.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Designers of high-end multichannel audio systems have a new industry standard analog volume control integrated circuit: the CS3318 from Cirrus Logic. The flagship CS3318 is an eight-channel, high-voltage, digitally controlled analog volume control IC that is the benchmark for audio quality, showcasing 127 dB dynamic range.

The CS3318 operates from a ±9 V power supply, with 118 dB adjustable gain ranging from +22 dB to –96 dB, negligible distortion, and excellent inter-channel isolation. Plus, a 0.25 dB step size with zero-crossing detection and programmable time out ensures remarkably smooth control of volume adjustment. The CS3308 is a pin-compatible ±5 V version with a very high dynamic range of 123 dB.

Both the CS3318 and CS3308 reduce external component count and printed circuit board space, helping OEMs achieve more compact products at a lower cost. Patent-pending technologies, such as dynamic address assignment and simultaneous master volume controls across multiple devices over a single serial control bus, simplify designs and further reduce costs.

Applications

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- Digital mixing consoles
- Outboard audio converters
- PC soundcards
- External audio interfaces
- DSP amplifiers and in-car entertainment systems

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modules provide optical isolation to as much as 4000V. The board operates at 5V or with a selection of dc/dc-converter options that allows an input-voltage range of 9 to 75V. The Opto104 costs $375 in single quantities.

BRING ON BANDWIDTH

Even with an expanded footprint, the data rates of many newer applications exceed the limitations of shared-bus systems. In these high-speed applications, which handle imaging or other signal-processing problems, designers have adopted serial switched-fabric communications techniques to transfer data directly between subsystems. Because of its compatibility with driver and operating software, PCI Express has become the fabric of choice for PC-compatible systems. The technology's LVDS provides maximum bandwidth between nodes. The basic PCI Express link comprises two signal paths that use small differential-voltage swings and constant current-line drivers to communicate at a minimum of 2.5 Gbps in each direction. Low-voltage swings deliver low-noise signals at low power consumption. Designers can increase the bandwidth of an individual PCI Express link by simply adding signal pairs, or lanes, until they reach the desired performance level. The PCI Express specification supports one, two, four, eight, 16, and 32 lanes.

The EPIC Express standard extends PCI Express fabric technology to industrial embedded computers. Using the same board size as the standard EPIC platform, the Express version replaces the parallel-PCI-bus connectors with smaller, serial connectors that retain the stacking features of PC/104 architecture. The ISA connectors remain part of the specification to ensure compatibility with the thousands of legacy expansion modules. The new standard also defines a PC/104-sized EPIC Express module that you can stack with legacy modules. Unlike PC/104, the stacking order for EPIC expansion modules is significant. EPIC Express expansion modules must be closest to the base single-board computer with standard PC/104 modules on top. EPIC and EPIC Express are open hardware standards allowing designers to develop conforming boards without licensing fees or royalties. Complete implementation details and the EPIC Express specification are available for downloading from the EPIC Express Web site.

Although single-board computers and expansion modules based on EPIC Express are not yet available, the new standard promises to re-energize PC/104 design possibilities. Small-system designers will be able to combine the latest high-performance devices with off-the-shelf modules to simplify and shorten the embedded-development cycle. With the relentless flow of new technology and regulations (see **sidebar** "Coming down the pike"), a standard that integrates new capabilities into a popular embedded architecture deserves careful consideration. EDN

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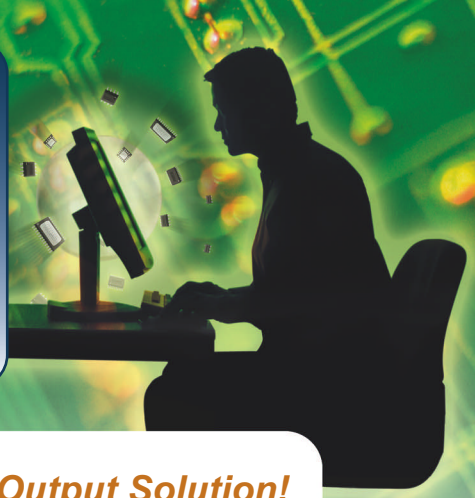

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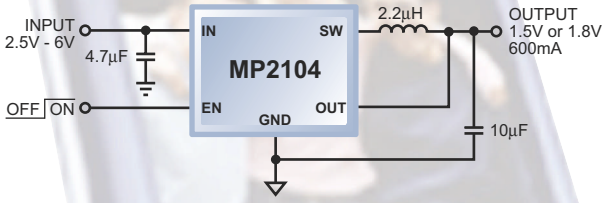

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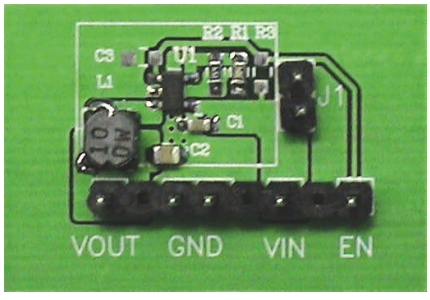

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MP2106	800kHz	2.6 - 15	1.5	QFN10 (3x3)
MP2305	340kHz	4.75 - 23	2.0	SOIC8
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Featured Non-Synchronous Bucks				
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MP2354	380kHz	4.75 - 23	2.0	SOIC8
MP1593	385kHz	4.75 - 28	3.0	SOIC8

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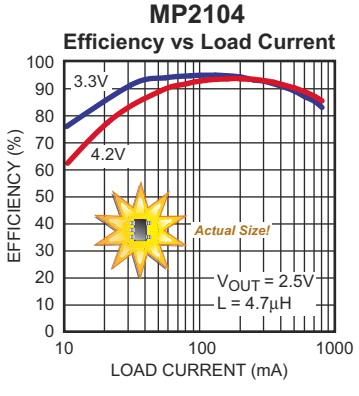

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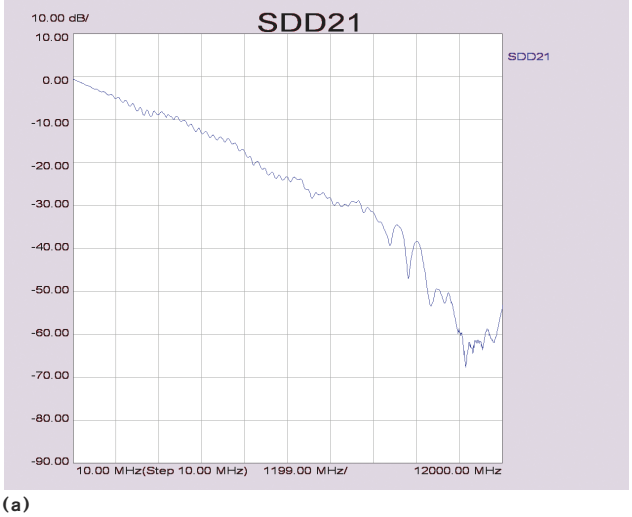
Digital and microwave worlds converge in 10-Gbps-backplane design and test

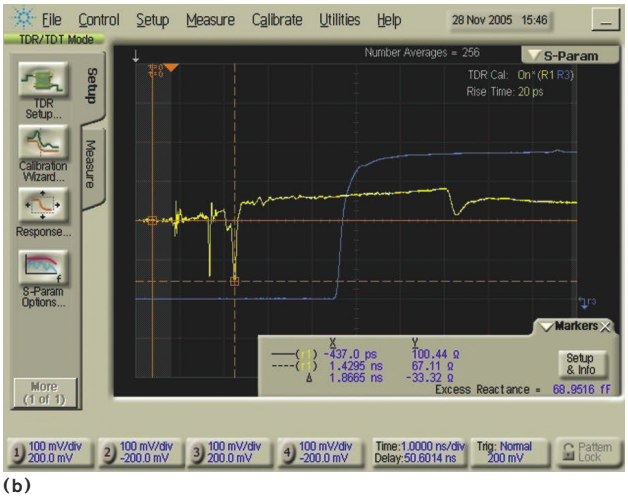
GETTING USABLE SIGNALS THROUGH BACKPLANES IS FAR FROM TRIVIAL WHEN SPEEDS REACH 10 GBPS. BY PREDISTORTING AND EQUALIZING SIGNALS, DRIVER AND RECEIVER ICs ALLOW THE USE OF LOW-COST SUBSTRATE MATERIALS, BUT GOOD DESIGNS ARE NO ACCIDENT.

Although you won't find them everywhere, communications systems that operate at 10 Gbps have been available for several years and are becoming more common. Architectures include copper cables with lengths of several meters and optical fibers with spans of tens or even hundreds of kilometers. When someone proposes transmitting 10-Gbps signals across a backplane in which the path is less than 1m long, you may expect the task to be manageable. However, when you consider signal-density requirements and impose realistic cost constraints, a different picture develops: You can no longer view the backplane as just a pc board to route signals; you must think of it as a complex communication system.

The basic blocks of a digital-communication system include the transmitter, the channel, and the receiver. Whereas it may seem unusual to consider a copper trace on a pc board as a communication channel, the attenuation, signal reflections, pulse dispersion, and intersymbol interference that a signal encoun-



(a)



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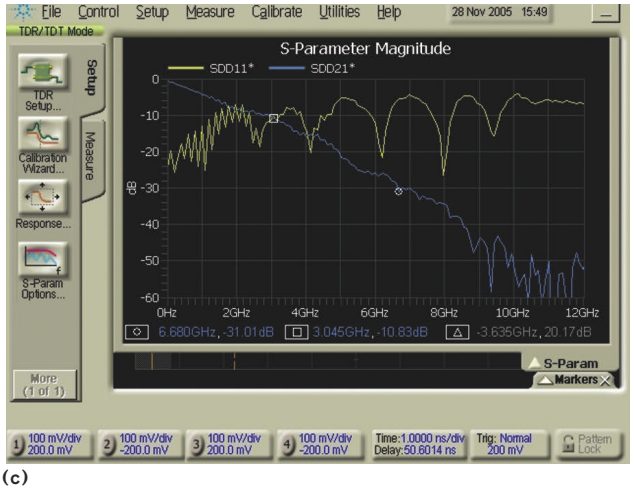


(c)

Figure 1 Backplane S_{21} bandwidth measurements compare the results of a VNA (a), a TDR trace (b), and the transformed TDR trace (c).

ters when traversing a 1m backplane rival the signal impairments in a 100-km optical link. To have any chance of successfully transmitting 10 Gbps through a backplane, you must understand and be able to overcome the degradation mechanisms that affect very-high-frequency signals traveling over and through common pc-board materials. The transmitted information may be digital, but the impairment phenomena are creatures of an analog—indeed, an RF/microwave—world.

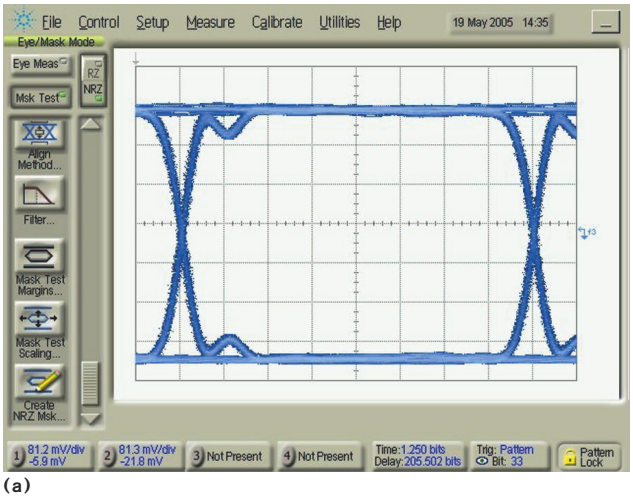
The desire to produce 10-Gbps backplanes stems from the ever-growing need to send more information at greater speeds to more places. Backplanes serve as the intersection and traffic control for complex communication systems. Given the cost constraints on high-speed backplanes, the types of materials that manufacturers can use are limited to FR-4 and similar board dielectrics. The frequency-dependent loss is significant. That is, the higher frequency components of a data stream experience more attenuation than do the lower frequency components. The amount of loss is also proportional to the length of any trace. That is, the loss through a 1m board is twice that through a 0.5m board. This loss can almost destroy a 10-Gbps signal as it traverses the channel.

HUGE CHALLENGE

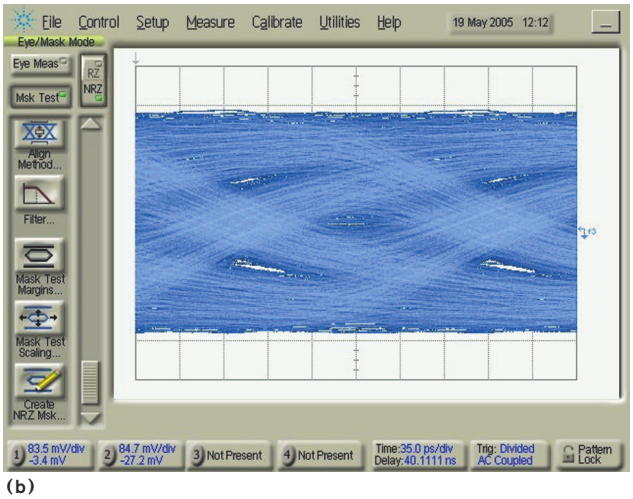
In addition to the severe degradation that the channel causes, a huge technical challenge awaits the designer of the transmitter and receiver chip sets. Backplane Ethernet applications are primarily enterprise-switch fabrics or computer servers providing 100 to 500 hot-swappable ports in a unit the size of a compact refrigerator. Such port densities require several custom ASICs, each having four to 200 embedded SERDES (serializer/deserializer) ports. These ASICs reside on eight to 12 densely populated, hot-swappable line cards that plug into the system backplane. This density and the requirement for a BER (bit-error ratio) of 10^{-17} demand per-port power of approximately 100 mW and ASICs that use 90-nm CMOS technology to achieve the requisite die size. Transmitted jitter can be no larger than a few picoseconds.

The backplane's limited performance is easiest to observe through a channel-bandwidth measurement. The result is effectively attenuation versus frequency. You commonly perform the measurement with a VNA (vector-network analyzer), which applies a known-amplitude sine-wave signal to the backplane, measures the output signal with a receiver tuned to the input-signal frequency, and displays the ratio of output to input. Designers commonly refer to the measured bandwidth as the S_{21} S (scattering)-parameter. The 2-1 notation indicates the ratio of the signal amplitude at Port 2 (the output) to that at Port 1 (the input). A TDR (time-domain reflectometer) can also measure the channel's output-to-input ratio, but instead of applying a swept-frequency sinusoid, the TDR applies a very-fast-edge step function as the input stimulus. To observe S-parameters, measurement software transforms the time information into the frequency domain (see **sidebar** "Going with the flow: S-parameters verify the performance of communications channels").

Figure 1 shows the S_{21} measurements of a 1m backplane. Designers performed one measurement with a VNA and the other with a transformed-TDR result. Although the results from the two instruments are similar, as they should be, the important point to observe is what frequencies are significantly attenuated. At less than 1 GHz, the signal decreases by 3 dB or is at 50% power. At about 5 GHz, the signal has been attenuated 20 dB or is at 1% power. The frequency content of NRZ (non-return-to-zero) data at 10 Gbps, at least at the transmitter output, has significant signal content where the backplane has 10 to 20 dB or more attenuation. This attenuation dramatically alters any data signal that appears at the backplane output. This effect is easiest to see by using a wide-bandwidth oscilloscope to view the data eye diagrams.



(a)



(b)

Figure 2 A 10-Gbps signal from a pattern generator (a) passes through a 40-cm FR-4 trace with devastating effects on the eye diagram (b).

It is obvious that, at a 10-Gbps data rate, the backplane bandwidth has a devastating effect on the eye diagram (**Figure 2**). The eye is completely closed. Without some help, a receiver's decision circuit will be unable to interpret the data and achieve a reasonable BER. Because making dramatic improvements to the backplane itself is likely to be expensive, the burden of system-level improvement falls on the transmitter and receiver. One critical aspect of the backplane's signal-degradation mechanisms is that they are systematic and predictable. This predictability opens the door to use of advanced communications schemes to correct the impairments. At least two possible approaches to this task exist. One is to predistort the transmitted signal—making

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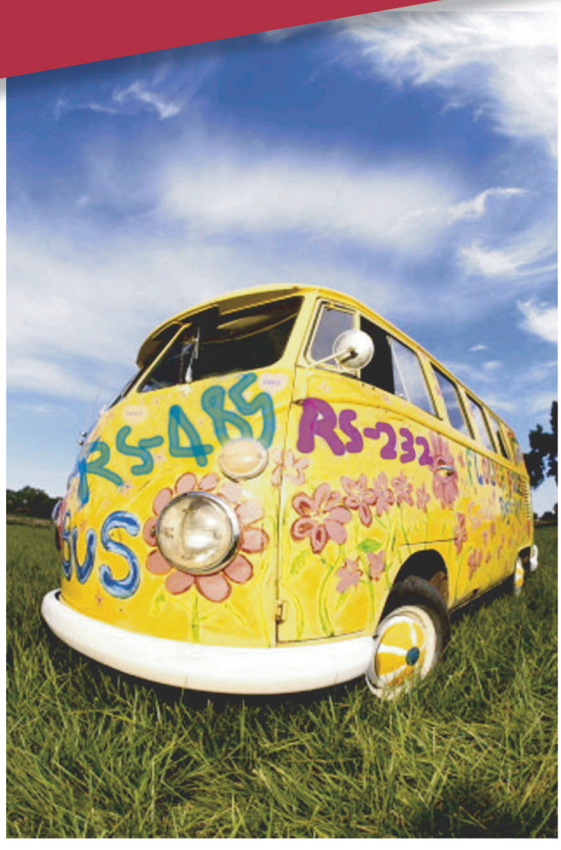

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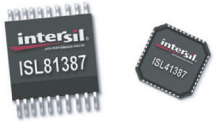

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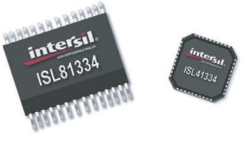

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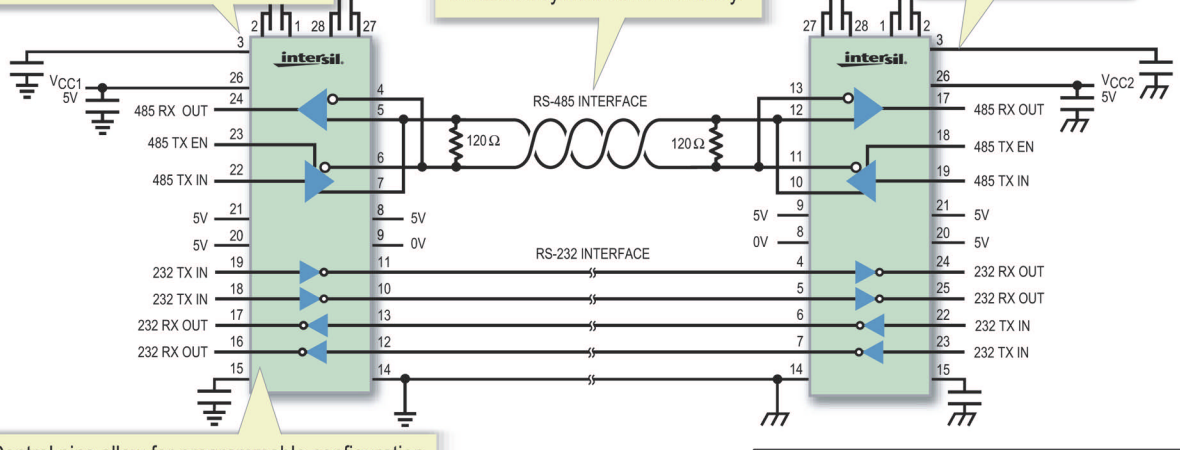

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the predistortion the inverse of the channel impairment. This technique is commonly known as de-emphasis. Another approach, equalization, corrects the signal impairment at the receiver. Ideally, predistortion at the transmitter or equalization at the receiver cancels out the channel's high-frequency attenuation. When the signal degradation is severe enough, you can use both transmitter de-emphasis and receiver equalization.

TRANSMITTER DE-EMPHASIS

Transmitter de-emphasis usually reduces the amplitude of the later portion of a logic 1 pulse and similarly increases the later level of the logic 0 pulse. Most predistortion schemes set the amplitude of the first one bit as the nominal amplitude (1V in 90 nm) and make the amplitude of the following bits adjustable. When driving long channels, the reduced amplitude of the trailing bits leads to reduced high-frequency content. For short channels, the amplitude of the trailing bits remains near the same amplitude as the leading bit. Note that when consecutive bits are identical—for example, a 0-1-1-1 sequence—only the first one following a zero has the boosted signal level. Adjacent ones have the unboosted nominal amplitude.

An intuitive basis for the effect of waveform emphasis is that high-frequency losses have a high impact on the edge of the signal and have little impact on the flat or nontransient regions of the data. Thus, the emphasis applies only to ones preceded by a zero and zeros preceded by a one. **Figure 3** compares a normal NRZ signal and its response at the backplane output. It also includes an emphasized NRZ signal from a parallel BERT (BER tester) and its backplane output. Note how transmitter emphasis has pried open an eye that would be closed for a common NRZ signal.

To improve a signal through receiver equalization, you must create a network whose response is the inverse of the backplane's. The receiver response should then cancel the channel response. You create a feedforward, or linear, equalizer by tapping off portions of the incoming signal and recombining the tapped signals with the original. Each tap has a delay and gain associated with its path leading to the summing node. Common designs usually have delay values of some fraction of the bit period. You can amplify or attenuate the tapped signals, and the approach uses both positive and negative tap values. To understand how the tap structure can correct for the channel response, a time-domain view of the channel response, rather than the frequency domain or S-parameter view, is helpful.

Although it is hard to see in the eye-diagram display, the closure of the eye is due to the sluggish response of signals passing through the channel. The trajectory of any bit is likely to be influenced by many of the preceding bits. For example, a logic 1 preceded by several consecutive 1s is much more likely to reach its ideal amplitude than a logic 1 preceded by several consecutive 0s. A 1 preceded by 1-0-1-0 will have another unique trajectory. You can see how a given bit influences others by viewing its impulse or pulse response.

EQUALIZER DESIGN

The limited bandwidth of the channel leads to broadening of the impulse response (**Figure 4**). Note also that some ringing in the response in this case continues for several bit peri-

GOING WITH THE FLOW: S-PARAMETERS VERIFY THE PERFORMANCE OF COMMUNICATIONS CHANNELS

As digital-communications signals extend well into gigabit-per-second rates, you can no longer view the pc-board traces that carry those signals as simple connections from Point A to Point B. Signal wavelengths are shorter than traces, and transmission-line theory helps in understanding how these signals propagate. Measurement techniques that RF/microwave engineers have used for decades are now important to high-speed-digital-design engineers. In particular, S-parameter measurement techniques are becoming common as transmission rates increase.

S, or "scattering," parameters describe how energy flows in a network. One common S-parameter, S_{21}, where 2 represents the point at which energy exits the channel and 1 represents the point at which energy enters the channel, describes how well energy flows from one end of a channel to the other. S_{21} is the ratio of the output signal to the input signal. The measurement is a function of frequency. Thus, a power amplifier's S_{21} measures the device's gain versus frequency, from which you could obtain the amplifier's bandwidth. S_{21} of a cable could be a measure of attenuation versus frequency, because cables tend to have increased loss as frequencies increase.

It can be difficult to launch high-frequency energy into a network. It is not uncommon for energy to reflect back toward the original source. Keep in mind that a reflected signal can show up at unexpected places or times and can degrade communications quality. S_{11} describes this effect, in which energy travels into a component or channel port and the energy that reflects back is measured at the same port that it went into. S_{11} is the ratio of the reflected energy to the input energy. Generally, S_{11} should be low, indicating small reflection levels. S_{22} describes how reverse-flowing signals reflect off a device's output port. Designers have historically used network analyzers to measure S-parameters. Network analyzers use as the stimulus a sine-wave signal generator that can operate over a wide range of frequencies. A receiver the can measure the response–the output or reflected signal–makes up the other half of the instrument. Engineers now also use time-domain reflectometers to generate S-parameter information through mathematically transforming measured time results into the frequency domain.

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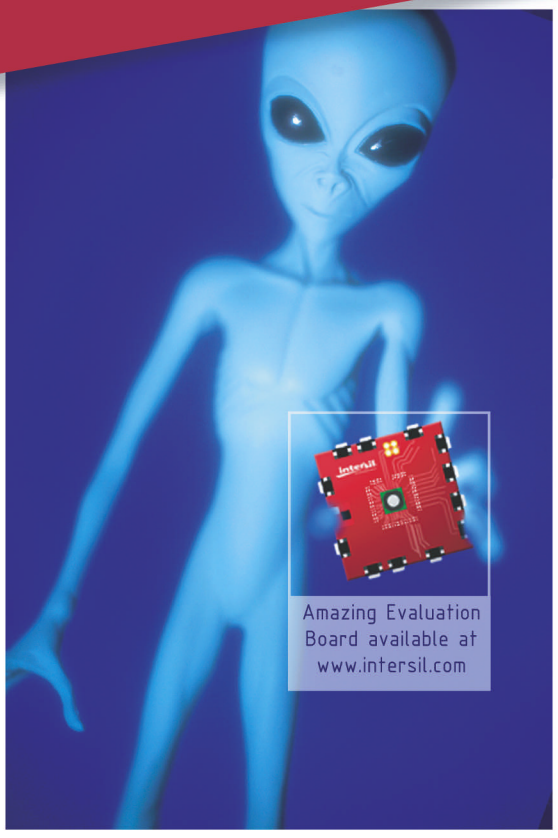

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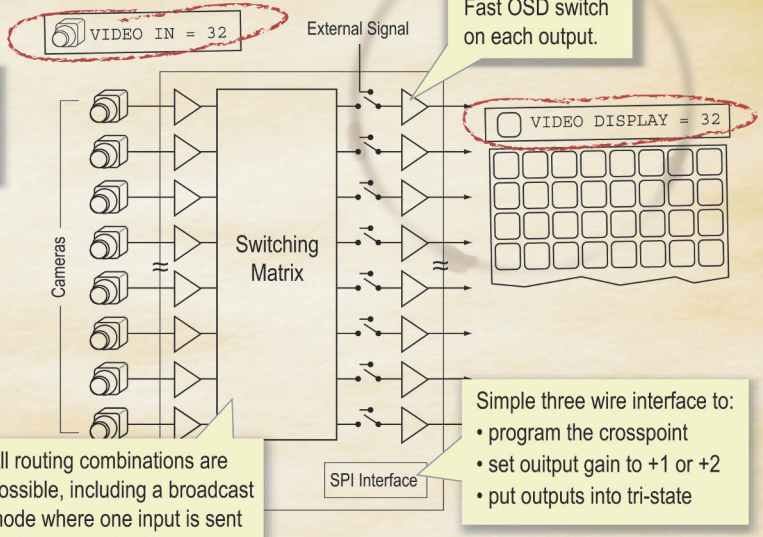

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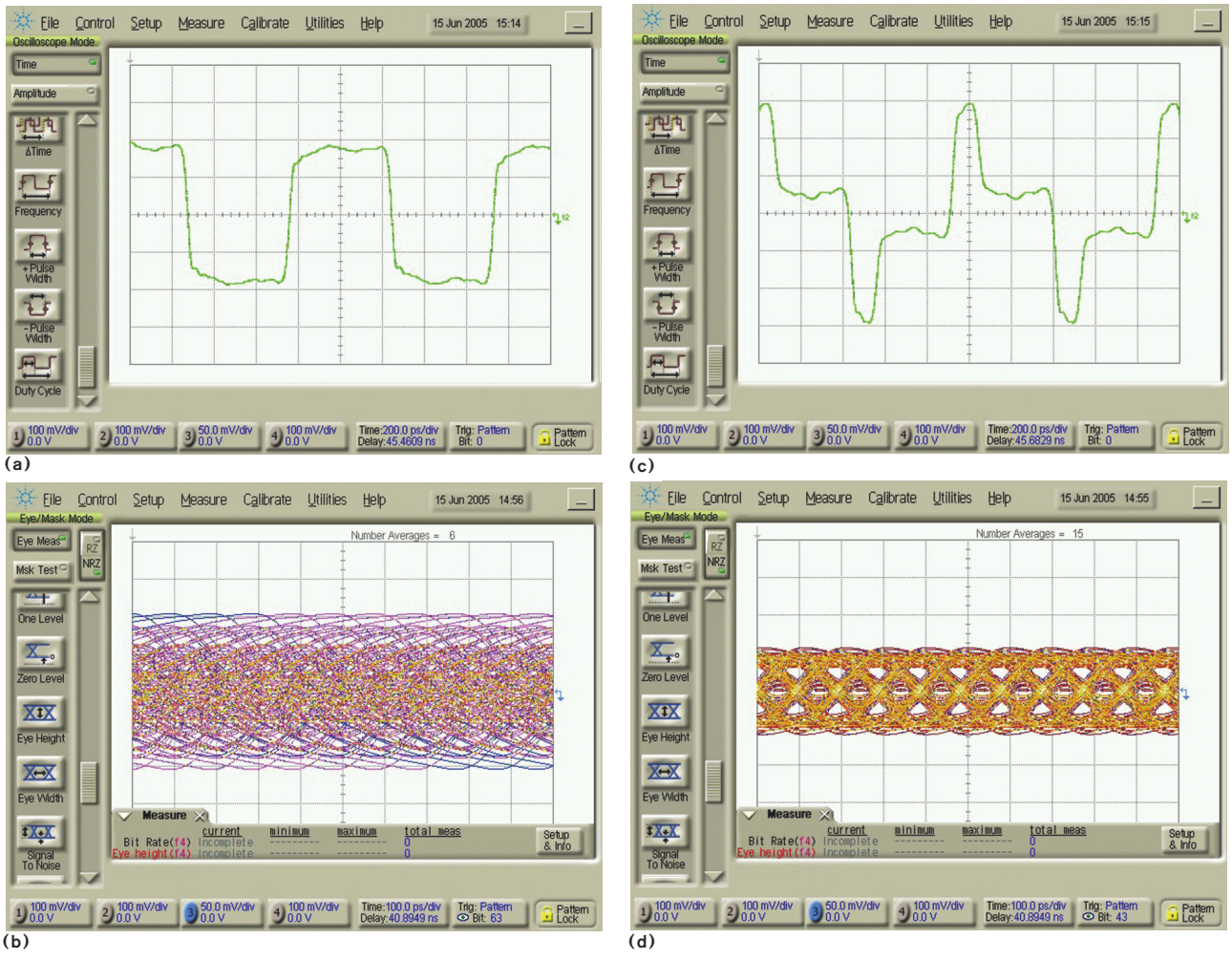

Figure 3 A parallel BERT has ordinary and de-emphasized waveforms (a and c) and the corresponding results (b and d) at the output of a 1m backplane channel.

ods after the initial pulse. The combination of a broadened pulse and ringing beyond the period of a bit leads to degradation of the bits that follow in the data stream, and you can observe this degradation in the eye diagram as eye closure. In the equalizer, signals from the taps complement the impulse response. For example, if an undershoot occurs after the main pulse half a bit period away, a tap of the same amplitude but opposite in phase and a delay of half a bit period negate the undershoot. Adding other taps compensates for the remaining components of the pulse response. A four-tap linear equalizer achieves a relative signal improvement (**Figure 5**). For mechanical robustness, connectors have through-hole drilling of the backplane board. This approach leads to a via-to-stripline stub—effectively, a short transmission line. The stub can lead to a channel-impulse response that ripples and does not settle out until as long as 15 bit periods. This approach has some significant implications on the receiver's design.

Some backplanes have S_{21} responses that indicate a relatively wide frequency response, whereas others have narrower bandwidth. You would expect the backplane with the wider bandwidth to provide the better channel. However, the channel S_{21} describes only one part of the overall channel characteristic. The channel also interacts with the transmitter and the receiver. Nonideal impedances can cause signal reflections and re-reflections that may yield a complex impulse response that a simple S_{21} measurement of the channel may not expose. The overall impulse response may have ripples that extend beyond those for which an economical equalizer or de-emphasized transmitter can compensate. Channels with poorer frequency response may have better interaction with the transmitter and receiver and achieve a better system response than wider-bandwidth channels. Thus, predicting when a channel will work and when it will not may be difficult to accomplish solely through frequency-response measurements.

A receiver with a linear equalizer and a transmitter with de-emphasis may be insufficient to compensate for a complex backplane. You can achieve additional signal correction with a DFE (decision-feedback equalizer) at the receiver, usually following a linear equalizer. The DFE dynamically adjusts the receiver decision threshold rather than tries to manipulate the incoming signal. Thus, as the logic 1s become low or the logic 0s stray high, the decision threshold shifts accordingly and corrects decisions. The DFE also has signal taps to determine where the threshold should be. The more taps the DFE uses, the greater the level of signal corruption for which it can compensate. However, because previous decisions affect future decisions, a mistake by the deci-

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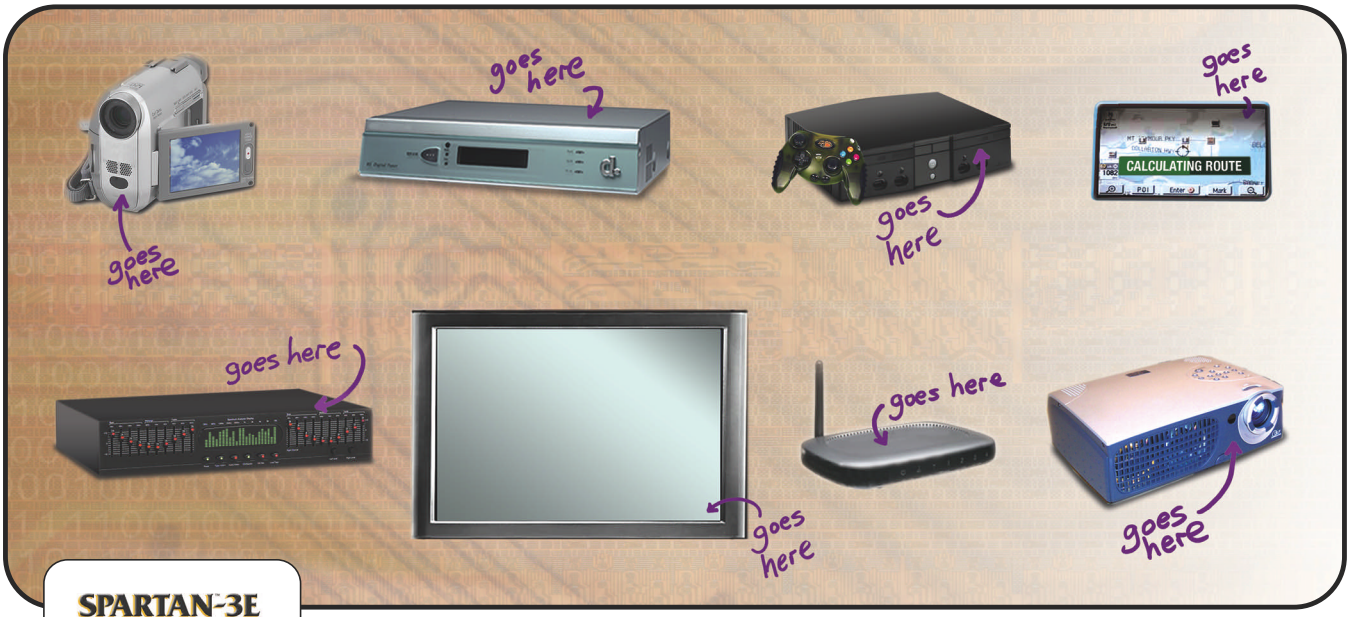

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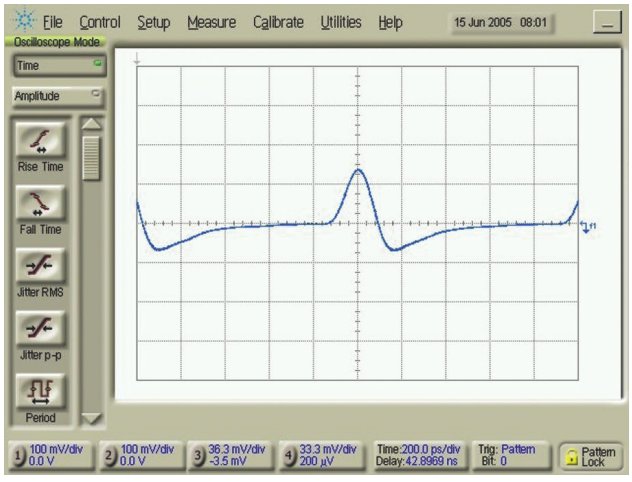

Figure 4 The impulse response shows some pulse broadening due to the limited bandwidth of the channel.

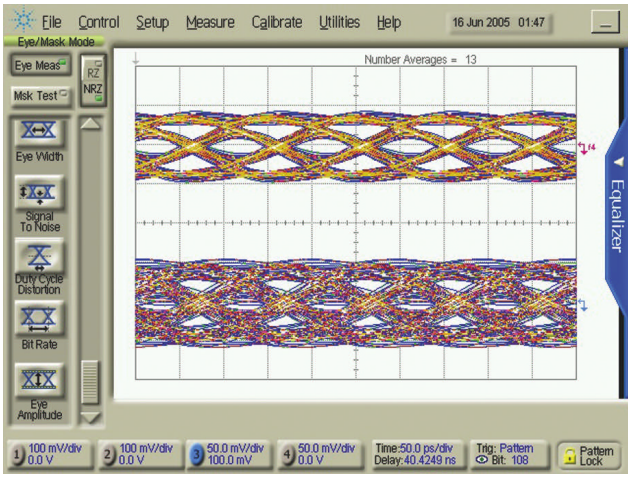

Figure 5 At the output of a 20-in. backplane, the upper eye diagram has passed through a virtual four-tap linear equalizer implemented within the digital-communications analyzer (oscilloscope).

sion circuit can lead to several incorrect bits. The more taps that exist, the longer it takes in bits for a mistake to clear out. Thus, an impulse-response ripple as long as 15 bits can lead to an impractically complex receiver-equalization design.

At high data rates, it can be difficult to constrain all of the signal energy to propagate through just the connectors and board traces. Channels can and usually do behave as antennas and radiate some of the signal power. Similarly, the antenna effect also works in the receiver mode. That is, the antenna picks up and propagates stray radiated signals, along with the intended signals, to a receiver. Because most backplanes have a multitude of simultaneously operating channels, the issue of channel crosstalk is critical. Crosstalk-measurement schemes verify how poorly channels radiate, as well as how susceptible channels are to radiated signals. The issue of crosstalk is not new and is a problem even for older, lower speed backplanes. The biggest contributors to crosstalk in backplane applications are often the connectors. A 10-Gbps "aggressor" signal's power can approach a "victim" signal's power at the 10-Gbps signal's 5-GHz Nyquist frequency. You must test the receiver for interference tolerance to prove that it is robust in the backplane environment.

DIFFERENTIAL SIGNALING

Differential-signaling schemes can reduce the level of signal radiation. The fields from the complementary signals can cancel each other out and reduce the overall radiation. From the receiver perspective, when signals do invade a channel, the same signal is present on both lines of a differential channel. A receiver with high common-mode rejection can better deal with crosstalk signals. The challenge for the very-high-speed backplane is that, because of cost constraints, a larger burden falls on the receiver to correct crosstalk problems. New receiver designs are necessary to yield higher degrees of tolerance to invasive signals.

The system's required ultrahigh data integrity necessitates intelligent failure prediction and good debugging information. In response to these requirements, some ASIC vendors provide built-in channel-signal-integrity analysis and performance tuning that provide both insight into the quality of the signal that the receiver sees and the ability to tune the transmitter and receiver to quickly detect and repair marginal interconnects and voltage or temperature anomalies.

Separate vendors may independently manufacture and test transmitters, connectors, pc boards, and receivers. This fact complicates the construction of a working design. Different backplanes may present a wide range of responses, and a one-size-fits-all design is likely to be insufficient for many channels. Trace geometries and layouts, material variance, and stub designs can lead to many levels of channel performance. Yet, system integrators expect the system to work when all of its components are assembled. The task of specifying the elements to guarantee a system-level specification can become difficult. Also, compensation schemes at the transmitter and receiver may need to be adaptive to allow usage with a broad range of backplane channels and connectors. Nevertheless, with several standards bodies tackling the problem, you can expect to soon see backplanes operating at 10 Gbps.

AUTHORS' BIOGRAPHIES

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Power Management for Portable Products

High Performance Analog Solutions from Linear Technology

Today's handheld portable products have even more features integrated, enabling them to inch closer to being all-in-one devices for tech-hungry consumers. However, this high level of integration presents a number of challenges for the system designer: accurate battery charging, autonomous power management (i.e. how to efficiently power the load when various input sources such as USB ports and AC adapters are present), efficient and bright display lighting and low noise, thermally efficient regulation. Linear Technology has developed products to meet these functional demands: full-featured battery management ICs featuring battery chargers and PowerPath™ controllers, inductorless, low-ripple multidisplay LED drivers and low noise, miniature footprint very low dropout regulators (VLDOs).

Single IC USB Power Manager, Ideal Diode Controller & Battery Charger in Compact 12mm² Footprint

The LTC®4085 is a monolithic autonomous power manager, ideal diode controller and standalone battery charger for portable USB devices in a 3mm × 4mm DFN package. It features PowerPath control which provides power to the USB peripheral device and charges a single-cell Li-Ion/Li-Polymer battery from the USB V_{BUS} or a wall adapter power supply if the adapter is present. It allows the end product to operate immediately when plugged in, regardless of the battery's state of charge. To comply with USB current limit specifications, the LTC4085 automatically reduces battery charge current as the system load current increases. Accurate programmable current limits maximize the power available from the USB port. To ensure that a fully charged battery remains fresh when the bus is connected, the IC directs power to the load through the USB bus rather than extracting power from the battery. Once the power source is removed, current flows from the battery to the load through an internal 200mΩ low loss ideal diode, minimizing voltage drop and power dissipation. Onboard circuitry is provided for an optional external PFET hookup to reduce the overall ideal diode impedance below 50mΩ, if required by the application.

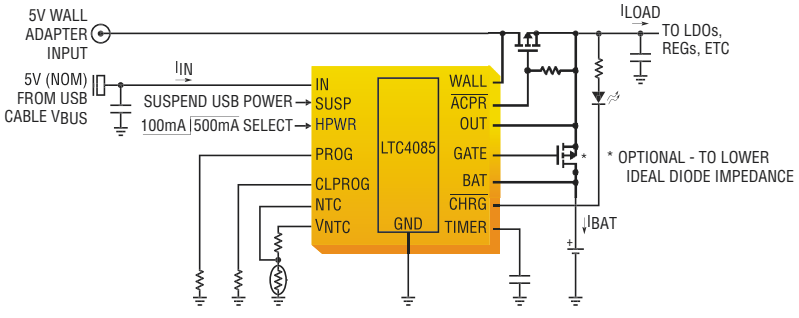


Figure 1. LTC4085 USB Power Manager

PowerPath Control and a Low-Loss Ideal Diode

With the LTC4085, the system load always has priority to receive the input power, while the remaining current goes to charge the battery. The LTC4085 is designed to receive power from a USB source, a wall adapter or a battery. It can then deliver power to an application connected to the OUT pin and to a battery connected to the

Power Management for Portable Products

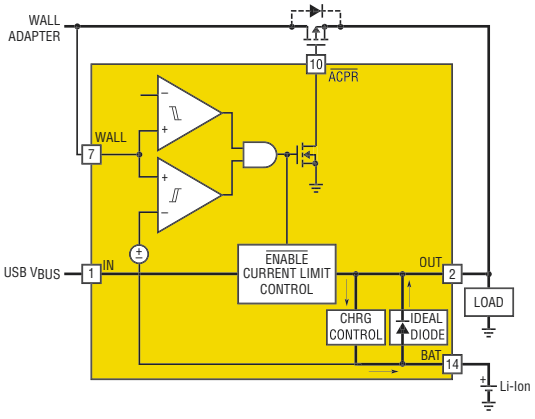


Figure 2. LTC4085's PowerPath Control Simplified Circuit

BAT pin (assuming that an external supply other than the battery is present). See Figure 2 for details.

An ideal diode function provides power from the battery when the output/load current exceeds the input current limit or when input power is removed. Powering the load through the ideal diode instead of connecting the load directly to the battery allows a fully charged battery to remain fully charged until external power is removed. Once external power is removed, the output drops until the ideal diode is forward biased. The forward biased ideal diode then provides output power to the load from the battery.

The LTC4085 also has the ability to receive power from a wall adapter. Wall adapter power can be connected to the output (load side) of the LTC4085 through an external device such as a power Schottky or FET, also shown in Figure 2. The LTC4085 has the unique ability to use the output, powered by the wall adapter, as a path to charge the battery while providing power to the load.

Multidisplay LED Driver Features 600mA Output Current and 95% Efficiency

The LTC3209-1/-2 are highly integrated, 850kHz, low noise, high efficiency multimode charge pumps for driving Main, Camera and Auxiliary LED displays in cellular phones. They can each drive up to eight LED current sources at up to 600mA of total output current. The LTC3209-1 can drive up to a six LED Main display, a single LED Camera display, and a one LED Auxiliary display; whereas the LTC3209-2 can drive up to a five LED Main display, two LED Camera display and a one LED Auxiliary display, all from a compact 20-lead 4mm x 4mm QFN package. Each display has digital control with independent dimming and programming via a two-wire I²C™ serial interface. The LTC3209-1/-2's input voltage range of 2.9V to 4.5V has been optimized for single cell Li-Ion cellular applications. Constant frequency operation enables low ripple performance. Efficiencies when driven from a Li-Ion battery (3.6V nominal) reach 94% with quiescent current of only 400µA, maximizing battery run-time. Both the LTC3209-1/-2 require only four small capacitors and one resistor to create a tiny, low profile (<25mm², 0.75mm high) solution footprint.

No Ballast Resistors Necessary

The LTC3209-1/-2, unlike alternatives, features individual driver outputs for Camera, Main/backlight and Auxiliary displays. This eliminates the need for costly ballast resistors and provides more precise current sharing in multi-LED appli-

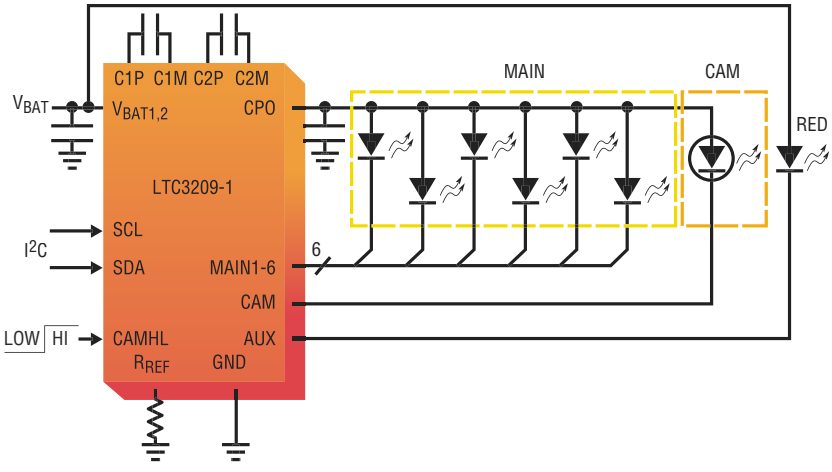


Figure 3. LTC3209-1 Typical Application Circuit

cations. In addition, it enables the total solution to be smaller, saving critical area in space-constrained portable applications.

High Efficiency, Multimode Operation

The LTC3209-1/-2 charge pumps feature low-noise constant-frequency operation and automatically optimize efficiency based on V_{IN} and LED forward voltage conditions. The devices power up in 1x mode and automatically switch to boost mode (1.5x) when any enabled LED current source approaches dropout; a subsequent dropout switches the parts into 2x mode. Maximum currents for the Main/CAM/Aux displays are set with a single resistor. LED currents are controlled with precision internal current sources while dimming and ON/OFF control for all displays are achieved via a 2-wire I²C serial interface. 256 brightness levels are available for the Main display, 16 for the CAM display and four for the AUX display. Internal circuitry prevents inrush current and excessive input noise during start-up and mode switching. In addition, the device has short circuit, thermal and open/short LED protection.

HIGHLIGHTS

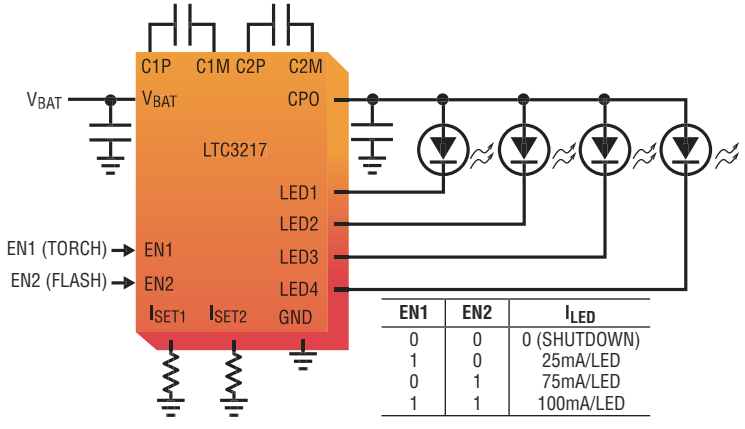
- **Up to 94% Efficiency without Inductors**
- **Multimode, Automatic Switching 1x/1.5x/2x Charge Pump for Optimal Efficiency**
- **Up to 600mA Total Output Current**
- **8 Current Sources Available as Main, Camera and Auxiliary LED Drivers:**
  LTC3209-1: 6 MAIN, 1 CAM, 1 AUX
  LTC3209-2: 5 MAIN, 2 CAM, 1 AUX
- **LED ON/OFF, Brightness Level Configurable Using 2-Wire I²C Interface**
- **Low Noise, Constant Frequency Operation**
- **4mm x 4mm x 0.75mm QFN-20 Package**

Cell Phone Camera LED Driver Features Low Noise and 92% Efficiency

The LTC3217 is a 900kHz, high efficiency multimode charge pump for driving multiple high current LEDs in cellular phone camera applications. Utilizing constant-frequency operation to enable low noise, it can drive up to four LED current sources at up to 600mA total output current, all from a compact 3mm x 3mm QFN package. Shutdown mode and current output levels are selected via two logic input pins. The LTC3217's input voltage range of 2.9V to 4.5V is optimized for single cell Li-Ion cellular applications. Efficiencies when driven from a Li-Ion battery (3.6V nominal) reach 92% with quiescent current of only 400µA, maximizing battery run-time. The LTC3217 requires only four small capacitors and two resistors to create a tiny, low profile (<25mm², 0.75mm high) solution footprint.

High Efficiency and Brightness Control Flexibility

The LTC3217 automatically optimizes efficiency based on V_{IN} and



EN1	EN2	I_{LED}
0	0	0 (SHUTDOWN)
1	0	25mA/LED
0	1	75mA/LED
1	1	100mA/LED

Figure 4. LTC3217 Typical Application Circuit

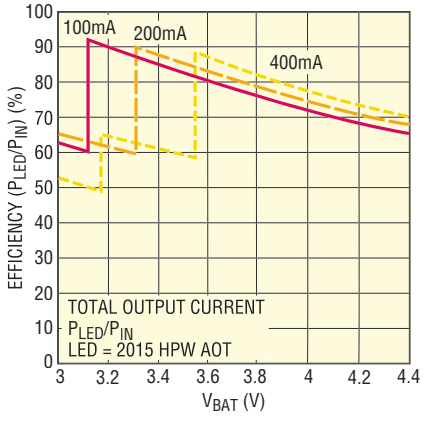


Figure 5. LTC3217 Multimode Efficiency Curves

Power Management for Portable Products

LED forward voltage conditions, featuring efficiencies above 92%. The device powers up in 1x mode and automatically switches to boost mode (1.5x) when any enabled LED current source approaches dropout; a subsequent dropout switches the part into 2x mode (see Figure 5).

The LTC3217 also features independent Torch and Flash I_{SET} and Enable pins. Three discrete current levels (high/medium/low) are available, selected via the EN1 and EN2 pins. The values of these currents may be programmed via the two I_{SET} resistors. LED brightness is controlled via pulse width modulation of the EN2 pin. The individual driver outputs eliminate the need for ballast resistors and provide more precise current sharing in multi-LED applications. Internal circuitry prevents inrush current and excessive input noise during start-up and mode switching. In addition the device has open/short LED protection.

300mA VLDO™ Operates Down to V_{IN} = 1.7V and Features 45mV Dropout

The LTC3035 is a 300mA very low dropout (VLDO) linear regulator with input voltage capability down to 1.7V. Featuring single-supply operation and a low adjustable output voltage range from 0.4V to 3.6V, it maintains extremely low dropout voltage of only 45mV at full load current. To allow operation at low input voltages, the LTC3035 includes an integrated charge pump converter that provides the necessary headroom for the internal LDO circuitry.

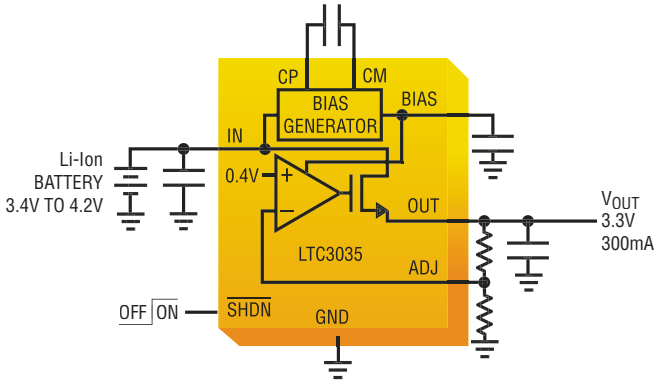


Figure 6. LTC3035 Typical Application Circuit

HIGHLIGHTS

- **Wide V_{IN} Range: 1.7V to 5.5V**
- **Low Dropout Voltage: 45mV Typical at 300mA**
- **Adjustable Output Range: 0.4V to 3.6V**
- **Built-In Charge Pump Generates NMOS Bias, No Need for External Supply**
- **±2% Voltage Accuracy over Temperature, Supply and Load**
- **Low Profile (0.75mm) 3mm x 2mm DFN-8 Package**

This low input voltage capability enables performance in numerous other applications such as Li-Ion or 2xAA alkaline cell to low-output voltage conversion systems. The LTC3035 features tight ±2% accuracy, low quiescent and shutdown currents of 100µA and 1µA, respectively, fast transient response and a small solution footprint with few external components. This makes it ideal for battery-powered handheld devices such as PDAs, cellular phones, media players, handheld medical and industrial instruments.

NMOS Power Device Enables Low Dropout Operation

Conventional LDOs integrate a P-type transistor (either PNP or PMOS) as the power pass device to deliver current from the input supply to its output. In contrast, the LTC3035 incorporates an NMOS transistor as its pass element in a source-follower configuration. This architecture provides several performance advantages over conventional P-type LDOs, including greater V_{IN} power supply rejection, lower dropout voltage and better transient response characteristics, while maintaining a smaller solution size.

LINEAR TECHNOLOGY

BY MICHAEL O'LOUGHLIN • TEXAS INSTRUMENTS

Advantages of interleaved boost converters for PFC

INTERLEAVING BOOST STAGES CAN REDUCE POWER-FACTOR-CORRECTED-PREREGULATOR POWER-CONVERTER INPUT- AND OUTPUT-RIPPLE CURRENTS THAT IN TURN REDUCE THE BOOST-INDUCTOR SIZE AND THE OUTPUT CAPACITOR'S ELECTRICAL STRESS.

The most popular topology for PFC (power-factor-corrected) preregulators is the boost converter, which has continuous input current that you can manipulate with average-current-mode-control techniques to force input current to track changes in line voltage. **Figure 1** shows a traditional single-stage boost. (To more easily explain the circuit operation, this article refers to dc inputs.) The change in inductor ripple current, ΔIL_1, is directly at the converter's input and may require filtering to meet EMI specifications. The diode output current, I_1, is discontinuous and requires the output capacitor, C_{OUT}, to filter it. In this topology, the output-capacitor ripple current, I_{COUT}, is high and is the difference between I_1 and the dc output current, I_{OUT}.

INTERLEAVING BOOST CONVERTERS

Figure 2 shows the functional diagram of a two-phase interleaved boost converter, which comprises two boost converters operating 180° out of phase. The input current is the sum of the two inductor currents, IL_1 and IL_2. Because the inductor's ripple currents are out of phase, they cancel each other out and reduce the input-ripple current that the boost inductors cause. The best input-inductor-ripple-current cancellation occurs at 50% duty cycle. The output-capacitor current is the sum of the two diode currents, I_1+I_2, minus the dc-output current, which reduces the output-capacitor ripple, I_{OUT}, as a function of duty cycle. As the duty cycle approaches 0, 50, and 100%, the sum

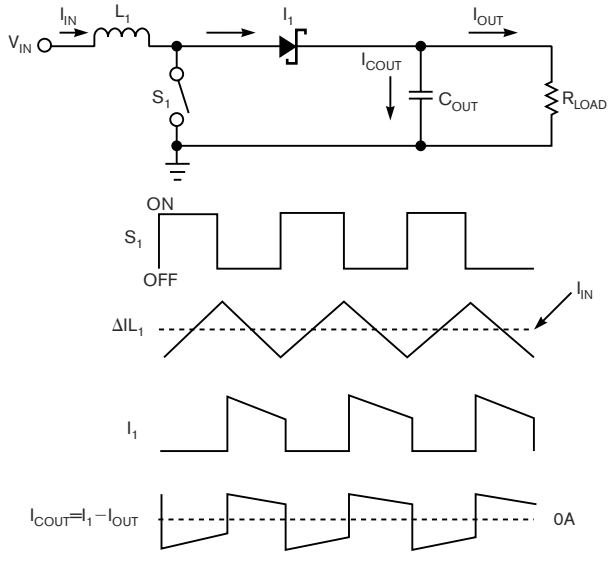


Figure 1 Input-ripple-current requirements to make EMI filtering easier limit a traditional PFC boost converter's inductor size. The traditional boost converter also has discontinuous output current that increases electrical stress on the output capacitor.

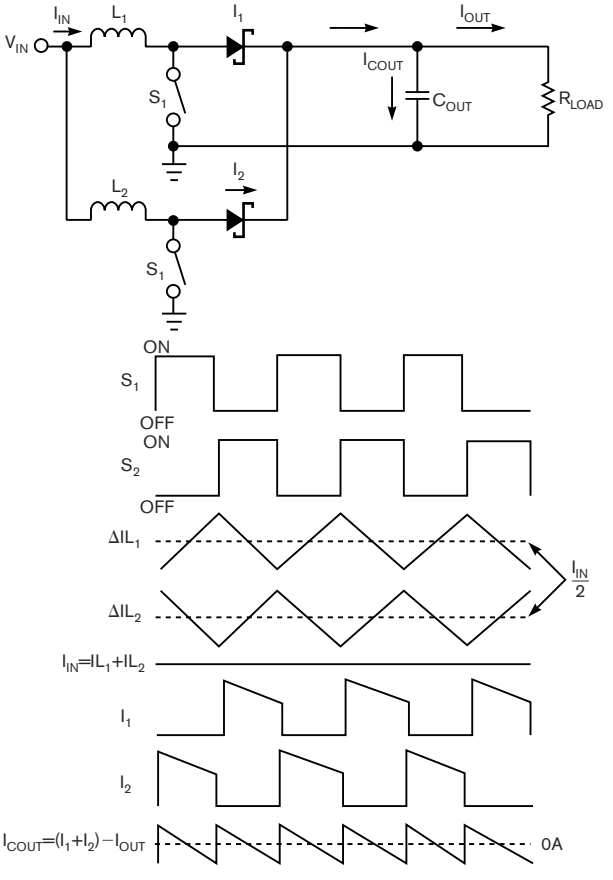


Figure 2 The interleaved boost converter consists of two boost converters operating 180° out of phase.

of the two diode currents approaches dc. At this point, the output capacitor has to filter only the inductor-ripple current.

INPUT-RIPPLE-CURRENT REDUCTION

The following **equations** and **Figure 3** show how the ratio of input-ripple current to inductor-ripple current, K(D), varies with changes in duty cycle. It is important to remember this variance when selecting inductors for the interleaved boost converter.

$$K(D) = \frac{\Delta I_{IN}}{\Delta IL_1}.$$

$$K(D) = \frac{1-2D}{1-D} \text{ IF } D \le 0.5.$$

$$K(D) = \frac{1-2(1-D)}{1-(1-D)} \text{ IF } D > 0.5.$$

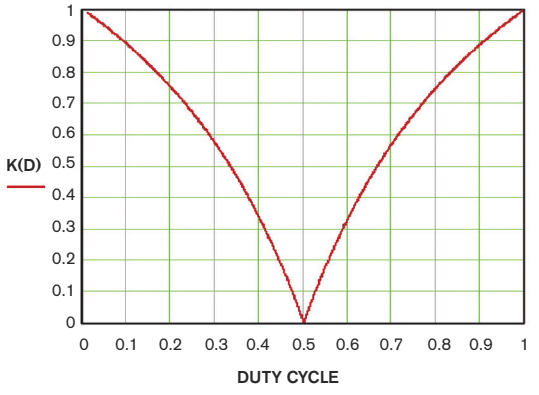


Figure 3 K(D), the ratio of input-ripple current to inductor-ripple current, varies with changes in duty cycle (D).

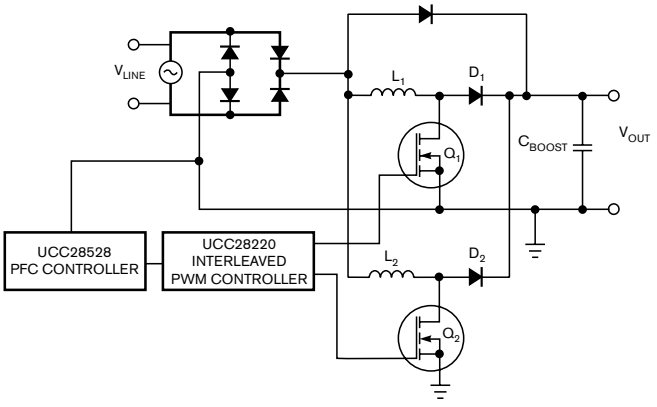


Figure 5 I evaluated the benefits of interleaving a 350W, two-phase preregulator.

Figure 4 shows the normalized output capacitor rms current in a single-stage boost converter, $I_{COUT\_rms\_single}(D)$, and the normalized rms current in a two-stage interleaved boost converter, $I_{COUT\_rms}(D)$, as a function of duty cycle. The **figure** demonstrates that the output-capacitor-ripple current in a two-phase interleaved boost converter is roughly half that of a traditional single-stage boost converter, reducing the electrical stress on the output-filter capacitor.

$$I_{COUT\_RMS\_SINGLE}(D) = \sqrt{(1-D)\times[1-(1-D)]}.$$

$$I_{COUT\_RMS}(D) = \frac{1}{2}\sqrt{2(1-D)\times[1-2(1-D)]} \text{ IF } D \ge 0.5.$$

$$I_{COUT\_RMS}(D) = \frac{1}{2}\sqrt{2[(1-D)-0.5]\times[1-2[(1-D)-0.5]]} \text{ IF } D < 0.5.$$

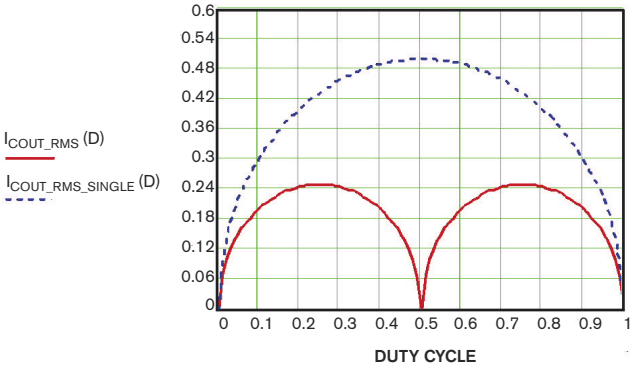


Figure 4 The output-capacitor-ripple current in a two-phase interleaved PFC boost preregulator is roughly half that of a traditional single-stage boost preregulator.

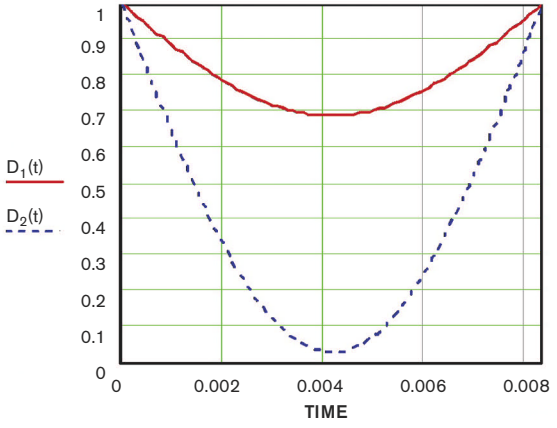


Figure 6 The duty cycle in a PFC boost preregulator varies with line voltage, $V_{IN}(t)$. Function $D_1(t)$ shows how the duty cycle varies with changes in line when the input is at 85V rms. Function $D_2(t)$ shows how the duty cycle varies with a maximum input of 265V rms.

EVALUATING INDUCTOR SIZE

To evaluate the benefits of interleaving PFC preregulators' reduced boost-inductor size, I conducted a mathematical comparison between a single-stage and a two-phase boost preregulator (**Figure 5**). The design requirements were a maximum output power, P_{OUT}, of roughly 350W; a minimum line input, V_{IN-MIN}, of 85V rms; a maximum line input of 265V rms; and an estimated converter efficiency of 95%. The inductors have a switching frequency, f_S, of 100 kHz. The inductors have an input-ripple-current requirement of 30%, and the inductors of both topologies have the highest inductor-ripple currents that occur at the minimum input and maximum input current.

I selected the inductors for both designs based on the worst-case ripple current. For a converter for a universal input, this point occurs at the minimum ac input at the peak line voltage, with the converter operating at a minimum duty cycle of 0.67. **Figure 6** shows how the duty cycle varies with line voltage $V_{IN}(t)$. Function $D_1(t)$ shows how the duty cycle varies with changes in line when the input is at 85V rms. Function $D_2(t)$ shows how the duty cycle varies with a maximum input of 265V rms. When the converter is operating at a maximum input of 265V rms, the maximum inductor-ripple current occurs when the input voltage is at half the output voltage. As the line voltage approaches the output voltage, the duty cycle decreases, reducing the inductor-ripple current.

$$V_{IN(t)} = V_{IN}\sqrt{2} \times SIN(2 \times \pi \times 60\ Hz \times t).$$

$$D_1(t) = D_2(t) = \frac{V_{OUT} - V_{IN}(t)}{V_{OUT}}.$$

The inductor-ripple current in a single-stage PFC preregulator is evident at the converter's input. A single-stage PFC induc-

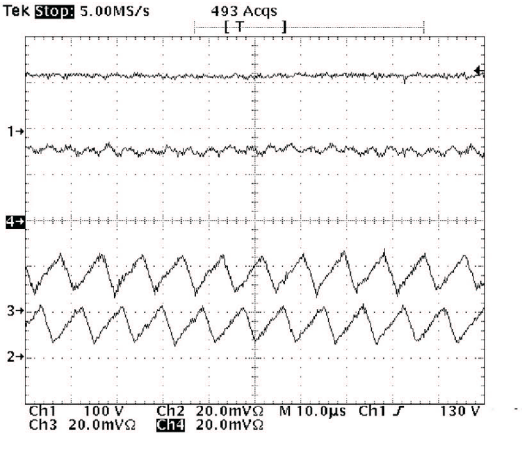
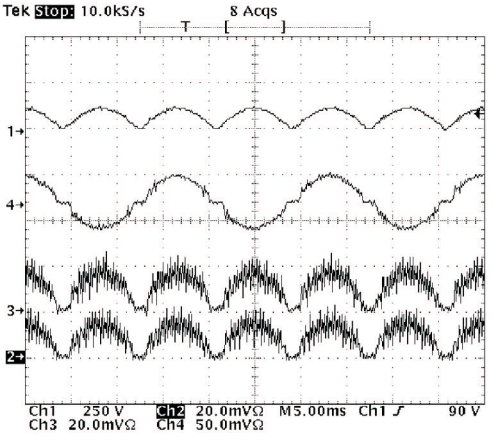
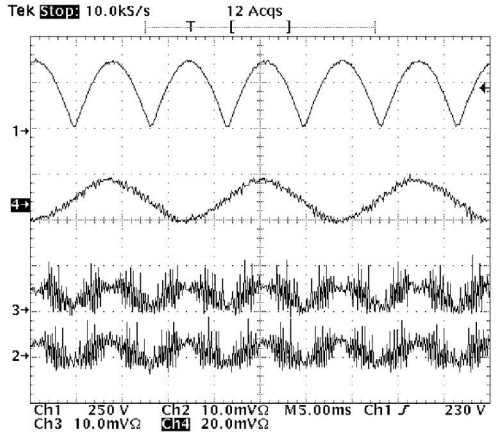


Figure 7 In this oscilloscope plot, CH_1 is the rectified line voltage, CH_2 is L_1 inductor current, CH_3 is L_2 inductor current, and CH_4 is input current. The current-conversion ratio is roughly 4A/division.



(a)



(b)

Figure 8 An oscilloscope plot shows the inductor currents of L_1 and L_2 with an input of 85V rms (a). Another plot shows the inductor current of L_1 and L_2 with an input of 265V rms (b).The channels on the oscilloscope plot are the same as those in Figure 7.

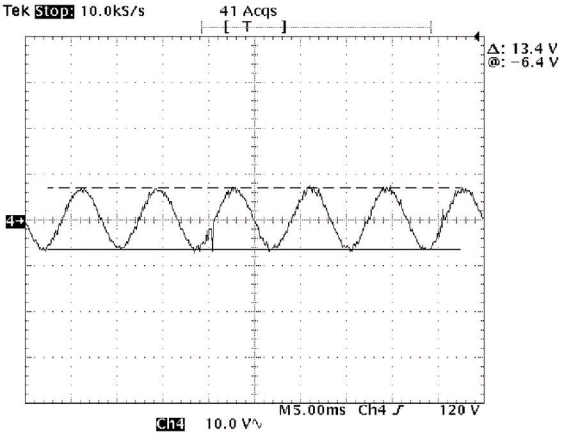


Figure 9 The oscilloscope plot shows the output-ripple voltage of the 350W prototype.

tor for a universal input would be roughly 450 µH. I based this calculation on where the inductor-ripple current was greatest at 85V rms input and 0.67 minimum duty cycle.

$$L_{SINGLE} = \frac{V_{INMIN}\sqrt{2} \times D_{MIN_{LL}}}{\frac{P_{OUT}\sqrt{2}}{V_{INMIN} \times 0.95} \times 0.3 \times f_S} \approx 450\ \mu H.$$

The dual-interleaved inductor has the same input-current-ripple requirements as the traditional preregulator. The change in inductor current in one of the interleaved boost stages is roughly 3.4A. Variable minimum duty cycle at the minimum rms input voltage requires an inductance of roughly 245 µH—about half the inductance a single-stage PFC preregulator at the same power level requires.

$$\Delta IL_1 = \frac{\frac{P_{OUT}\sqrt{2} \times 0.3}{V_{INMIN} \times 0.95}}{K(D_{MIN_{LL}})} \approx 3.4A.$$

$$L_1 = \frac{V_{INMIN} \times \sqrt{2} \times D_{MIN_{LL}}}{\Delta IL \times f_S} \approx 245\ \mu H.$$

LAB RESULTS

I evaluated a dual-interleaved boost converter using 200-µH inductors for L_1 and L_2 and the input current. The worst-case inductor-ripple current occurs when the converter operates at low input at the peak of the line. The oscilloscope plot in **Figure 7** shows the inductor currents of L_1 and L_2 with an input of 85V rms. CH_1 is the rectified line voltage, CH_2 is L_1 inductor current, CH_3 is L_2 inductor current, and CH_4 is input current. The current-conversion ratio is roughly 4A/division.

Figures 8a and **8b** show the input-line and inductor-ripple currents at maximum load. The channels of the scope plots are the same as in **Figure 7**. These waveforms clearly demonstrate a clean input-current waveform for Channel 4. This two-phase, interleaved-PFC design uses a 220-µF output capacitor. At full load for a single-stage, 350W PFC preregulator, the output-capacitor ripple would be roughly 33.5V. For a two-phase, interleaved PFC, the output ripple should be less than half of the single stage. The prototype's output-ripple voltage at full load is roughly 13V (**Figure 9**).

$$V_{RIPPLE} = \left(\frac{P_{OUT}}{V_{INMIN} \times 0.636} - \frac{P_{OUT}}{V_{OUT}}\right) \times \frac{1}{2\pi(2FLINE)C_{OUT}} \approx 33.5V.$$

Determining whether the prototype could meet current harmonic specifications EN61000-3-2 requires the prototype's input harmonics' full-load power. The first harmonic is the rms input current at 60 Hz. The proceeding harmonics are well within

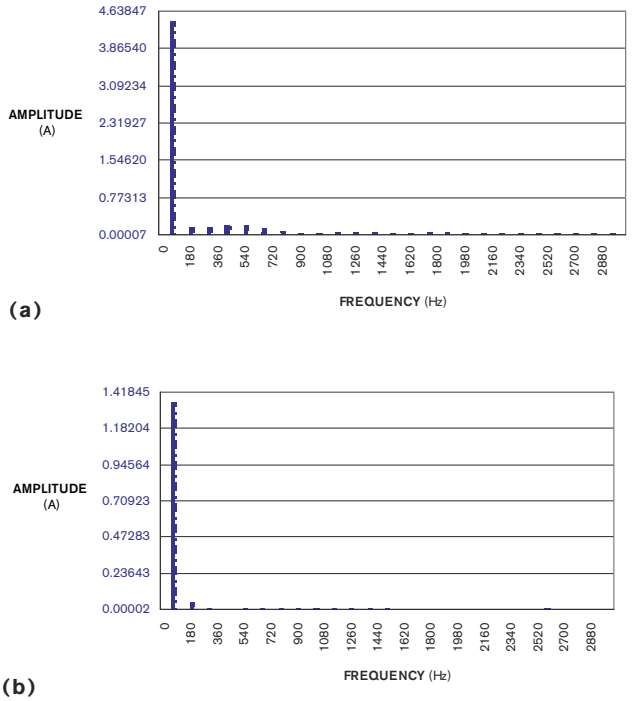


Figure 10 Input harmonics easily meet EN61000-3-2 Class D specifications. Figure 10a shows the rms harmonic-current content at low-line maximum output power. Figure 10b shows the rms harmonic-current content at high-line maximum output power.

CH61000-3-2 Class D specifications (**Figure 10**).

Interleaving PFC preregulators allows power-supply designers to reduce inductor magnetic volume. The inductor-ripple-current cancellation at the input of the power converter allows designers to reduce the inductance by roughly half. Interleaving also reduces the ripple current in the boost capacitor, alleviating electrical overstress on the output capacitor. With no filtering on the prototype circuit, the design achieves EN61000-3-2 Class D current-harmonic specifications. It has a slightly more complicated control scheme with a higher component count, but, in high-power applications, this trade-off is well worth it. EDN

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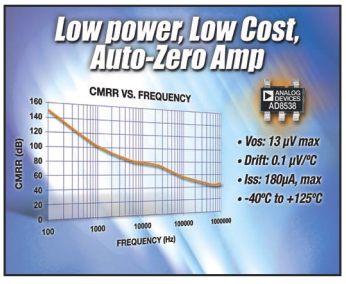
Currents Quarterly

Your First Look at New Analog and Mixed-Signal ICs from Analog Devices

Spring 2006

Extend Battery Life and Increase Accuracy in Portable Applications



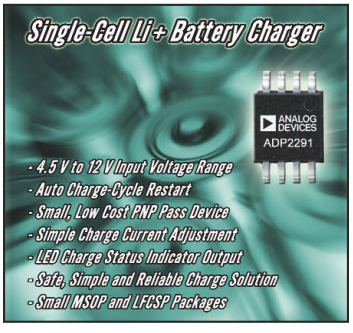
Designers of portable equipment require low power consumption levels to extend battery life. Often, this means sacrificing accuracy. The AD8538 requires a supply current of only 180 µA, while providing performance equivalent to products operating at over 1 µA of supply current. The AD8538 offers 13 µV maximum offset, 600 kHz bandwidth, and just 1 µV p-p of low frequency noise, enabling highly accurate and stable system designs without the size, complexity, and higher cost of solutions utilizing external autocalibration. The AD8538 operates from 2.7 V to 5.5 V and is specified from –40°C to +125°C.

AD8538 $0.89
www.analog.com/edncurrents

Get the Charge You Need at a Price You Can Afford with ADI's Compact, Low Cost, and Reliable Single-Cell Li+ Battery Charging System

With today's proliferation of portable battery-powered devices such as PDAs, MP3 players, and cell phones, it is becoming increasingly more important to select the proper battery charging solution. The ADP2291 is a constant-current/constant-voltage linear charger for a single-cell lithium ion battery, requiring just a few components to provide a simple and safe charging system that operates from a wide 4.5 V to 12 V input voltage range. It features an internally controlled, multistep charging cycle that improves battery life.

An external, low cost PNP provides the charging current to the battery and an external resistor sets the maximum charge current. A small external capacitor programs the maximum charge time. Additionally, the controller includes an LED driver to indicate the battery charging status.

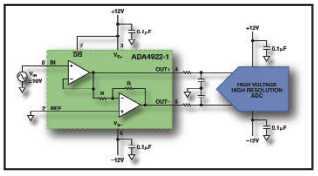


ADP2291 $1.12
www.analog.com/edncurrents

New Differential Amplifiers Simplify Driving 16-Bit to 18-Bit ADCs

Driving high resolution differential ADCs has typically required a number of external components, in addition to the amplifiers. Configured as easy to use, G = +2, single-ended-to-differential amplifiers, the ADA4941-1 and ADA4922-1 require no external components to drive 16-bit to 18-bit differential ADCs. Both devices offer high input impedance, as well as ultralow noise and distortion, which are essential for driving today's high resolution ADCs.

ADA4922-1: High Voltage, Low Distortion Differential Driver for 16-Bit to 18-Bit ADCs

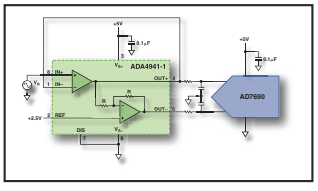


The ADA4922-1 differential driver is designed to directly interface with 16-bit to 18-bit ADCs that have input ranges up to ±20 V in a variety of applications including industrial instrumentation. Performing a single-ended-to-differential conversion with a fixed gain of 2, it features low noise (12 nV/√Hz), low distortion (–99 dBc at 100 kHz), and high input impedance (11 MΩ). Operating over a wide supply voltage (5 V to 26 V), the ADA4922-1 consumes 10 mA. Available in 8-lead LFCSP and SOIC packages, it is specified from –40°C to +85°C.

ADA4922-1	$3.59

www.analog.com/ednccurrents

ADA4941-1: Low Power, Low Noise Differential Driver for 16-Bit to 18-Bit ADCs

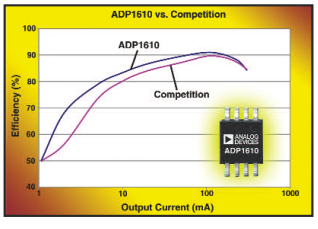


The ADA4941-1 is a differential driver with rail-to-rail outputs designed to directly interface with low power, 16-bit to 18-bit ADCs in a variety of applications including medical instrumentation and battery power systems. Performing a single-ended-to-differential conversion with a gain of 2, it features low noise (97 dB SNR at 100 kHz, V_o = 4 V p-p), low distortion (–105 dBc at 10 kHz), and high input impedance. An external resistive network can also be used for additional gain. Operating on +3 V, +5 V, or ±5 V supplies, the ADA4941-1 consumes only 2.1 mA. Available in 8-lead LFCSP and SOIC packages, it is specified from –40°C to +125°C.

ADA4941-1	$2.39

www.analog.com/ednccurrents

ADP1610/ADP1611: Dramatically Improve Battery Life for Portable Hand-Held Devices by Using ADI's Step-Up PWM DC-to-DC Controllers

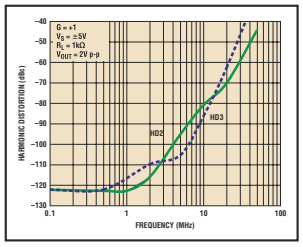


ADI's ADP161x family of step-up PWM dc-to-dc controllers offers design engineers a more efficient and cost-effective alternative to existing power hungry dc-to-dc controllers. The ADP161x family provides a consistently higher power efficiency rating through the full range of output currents as compared to other competitive solutions. Current mode control provides fast transient response to sudden load changes. These devices are offered in a popular, pin-compatible configuration that allows for hassle-free implementation in existing reference designs.

ADP1610	$1.25
ADP1611	$1.35

www.analog.com/ednccurrents

Ease Design Challenges of High Resolution Systems Requiring Low Levels of Noise and Distortion



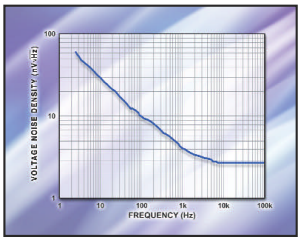
High resolution system design often requires performance trade-offs between noise and distortion. The ADA4899-1 is the industry's first unity gain stable op amp to achieve 1 nV/√Hz voltage noise and 16-bit to 18-bit distortion levels at 1 MHz (117 dBc SFDR). It features a patent-pending advanced circuit architecture that addresses these fundamental trade-offs, which are inherent in traditional input stages. In addition to the superior ac performance, the ADA4899-1 has dc input specifications of 0.23 mV maximum offset voltage and 1 μA maximum input bias current. For those applications with a high source impedance, the ADA4899-1 also features an input bias current cancellation mode, which reduces input bias current by a factor of 3100. The ADA4899-1 is available in a 3 mm × 3 mm LFCSP and an 8-lead SOIC package. Both packages feature an exposed metal paddle that enables a more efficient heat transfer from the IC to the PCB ground plane. The ADA4899-1 is rated to work over the extended industrial temperature range of –40°C to +125°C.

The ADA4899-1 is compatible with leading 16-bit to 18-bit ADCs, including the PulSAR® AD7674.

ADA4899-1	$1.89
AD7674	$30.92

www.analog.com/ADA4899

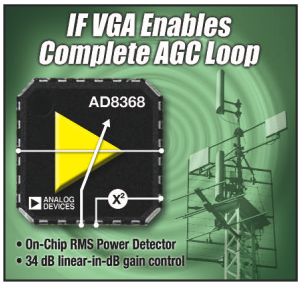
Lowest Noise, Precision Dual Amp for Low Voltage Applications



The AD8656's low noise (2.7 nV/√Hz) eliminates the need for discrete input stages or the use of multiple amps to lower system level noise in low voltage applications. 0.007% THD + N (total harmonic distortion + noise) improves SNR and accuracy for driving high resolution ADCs. These features—along with low offset and offset drift, 28 MHz bandwidth, and rail-to-rail input/output—are attractive for communications and audio applications as well as data acquisition systems and process controls. The AD8656 operates from 2.7 V to 5.5 V supplies and is specified from –40°C to +125°C.

AD8656 $1.10
www.analog.com/ednccurrents

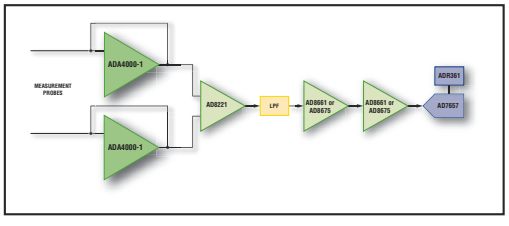
VGA Features High Linearity Over a Wide Frequency Range with Integrated On-Chip RMS Detector



Now you can have an analog-control, variable-gain amplifier (VGA) with exceptional linearity over a broad frequency range, perfect for your wireless infrastructure applications such as cellular base station radio transceivers. With a 3-dB bandwidth of 800 MHz independent of gain setting, a single-ended input and output drive, and exceptional linearity over the full operating range, the AD8368 is ideally suited for use in GSM, CDMA2000, W-CDMA, and TD-SCDMA cellular base stations. Operating from a single-supply voltage of 4.5 V to 5.5 V, the AD8368 consumes only 54 mA of current. The AD8368 is optimized to maintain a dynamic range of base station radio transceivers, ensuring that both weak and strong incoming call signals are effectively handled and maintained. In addition, the AD8368 simplifies and reduces the number of external components required by integrating an accurate root-mean-square (rms) power detector on-chip, which enables a complete automatic gain control (AGC) loop within a small 4 mm × 4 mm IC package.

AD8368 $4.55
www.analog.com/ednccurrents

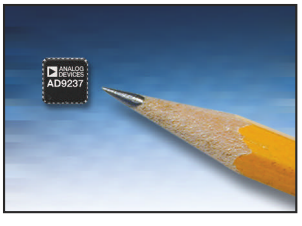
JFET Precision Amplifier Offers 75% Less Power Consumption in a TSOT-23



As the market moves towards lower power and higher board density, designers face lower power consumption requirements to reduce self-heating and the need for additional cooling with heat sinks and fans. The ADA4000-1 offers 75% less power consumption as well as 80% lower input bias current and 50% lower offset voltage at a lower price. It is offered in a 2 mm × 3 mm, 5-lead TSOT-23—saving board space and cost, and improving layout flexibility.

ADA4000-1 $0.91
www.analog.com/ednccurrents

12-Bit A/D Converter Consumes a Low 190 mW at 65 MSPS with No Compromise in Dynamic Performance

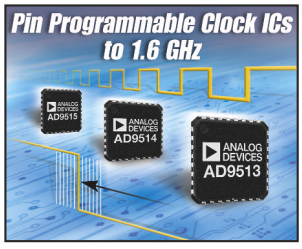


The AD9237 is a monolithic, single 3 V supply, 12-bit, 20 MSPS/40 MSPS/65 MSPS analog-to-digital converter with a high performance sample-and-hold amplifier and voltage reference. The AD9237 uses a multistage, differential pipelined architecture with output error correction logic to provide 12-bit accuracy at 20 MSPS/40 MSPS/65 MSPS data rates, and guarantees no missing codes over the full operating temperature range. The wide bandwidth, truly differential SHA allows for a variety of user-selectable input ranges and offsets, including single-ended applications. It is suitable for multiplexed systems that switch full-scale voltage levels in successive channels, and for sampling single-channel inputs at frequencies well beyond the Nyquist rate. With significant power savings over previously available analog-to-digital converters, and with its 66 dBc SNR performance, the AD9237 is suitable for applications imaging and medical ultrasound. A single-ended clock input is used to control all internal conversion cycles. The digital output data is presented in straight binary, twos complement, or gray code formats. An out-of-range (OTR) signal indicates an overflow condition, which can be used with the most significant bit to determine low or high overflow.

Fabricated on an advanced CMOS process, the AD9237 is available in a 32-lead chip scale package and is specified over the industrial temperature range (–40°C to +85°C).

AD9237 $7.00
www.analog.com/ednccurrents

Newest Member of 1.6 GHz Clock Distribution IC Family Includes Dividers, Delay Adjust, and Three Independent Outputs



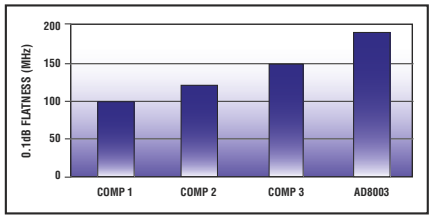
AD9513 $5.95

www.analog.com/ednc urrents

The AD9513, a member of the AD9515, AD9514, and AD9513 clock family, features a three-output clock distribution IC in a design that emphasizes low jitter and phase noise to maximize data converter performance. Other applications with demanding phase noise and jitter requirements also benefit from this part. There are three independent clock outputs that can be set to either LVDS or CMOS levels, which operate to output frequencies of 800 MHz in LVDS mode, and to 250 MHz in CMOS mode. Each output has a programmable divider that can be set to divide by a selected set of integers ranging from 1 to 32. The phase of one clock output relative to the other clock output can be set by means of a divider phase select function that serves as a coarse timing adjustment. One of the outputs features a delay element with three selectable full-scale delay values (1.5 ns, 5 ns, and 10 ns), each with 16 steps of fine adjustment. The AD9513 is ideally suited for data converter clocking applications where maximum converter performance is achieved by encode signals with subpicosecond jitter.

The AD9513 is available in a 32-lead LFCSP and operates from a single 3.3 V supply. The temperature range is –40°C to +85°C.

Drive High Resolution Video with a Triple 1.5 GHz Op Amp

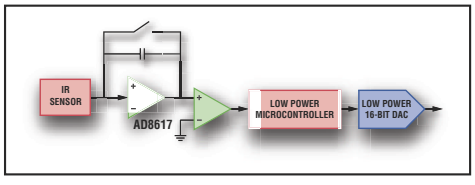


AD8003 $2.89
AD8000 $1.68

www.analog.com/ednc urrents

As video resolution and frame rates increase, the speed requirements of an amplifier become increasingly important. The AD8003 is a triple 1.5 GHz amplifier with a slew rate of 4300 V/μs. It offers designers 0.1 dB flatness of 190 MHz, 0.1% settling within 12 ns, and low differential gain (0.05%) and phase (0.01 degree) in an ultrasmall LFCSP package. The amplifier provides excellent dc precision with an input bias current of 7 μA typ and dc input voltage of 0.7 mV. The AD8000, a single version, is also available.

Low Noise, Low Power Op Amp for Low Battery Life Portable Applications

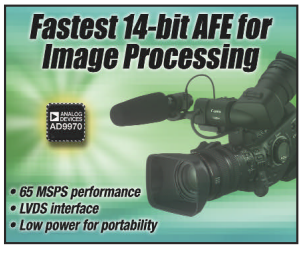


AD8613 $0.45
AD8617 $0.70
AD8619 $1.10

www.analog.com/ednc urrents

Power management and reliability are critical in portable medical and industrial applications. The AD8613/AD8617/AD8619 family of single, dual, and quad amplifiers delivers 50% lower noise and 30% lower power with twice the precision of competitive devices—a level of performance previously unavailable at comparable prices. Fully guaranteed low voltage operation down to 1.8 V makes the AD8613/AD8617/AD8619 ideal for battery-operated devices, such as temperature monitors and carbon dioxide detectors, where power management and reliability are critical.

Industry's Fastest 14-Bit Analog Front End Enables High Definition Image Processing Applications



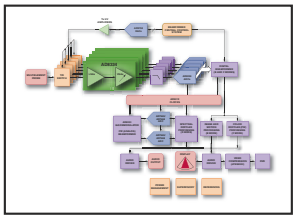
AD9970 $10.74

www.analog.com/ednc urrents

The AD9970 is a highly integrated CCD signal processor for high speed digital video camera applications. Specified at pixel rates of up to 62 MHz, the AD9970 consists of a complete analog front end with A/D conversion, combined with a programmable timing driver. The *Precision Timing*™ core allows adjustment of high speed clocks with 252 ps resolution at 62 MHz operation. The AD9970 also contains a reduced swing LVDS interface for the data outputs. The analog front end includes black level clamping, CDS, VGA, and a 62 MSPS 14-bit A/D converter. The timing driver provides the high speed CCD clock drivers for RG, HL, and H1 to H4. Operation is programmed using a 3-wire serial interface. Applications for the AD9970 include professional HDTV camcorders, professional and high end digital cameras, and broadcast cameras.

Packaged in a space-saving 5 mm × 5 mm, 32-lead LFCSP package, the AD9970 is specified over an operating temperature range of –25°C to +85°C.

Low Power Quad VGA Increases Image Resolution in Ultrasound Applications While Reducing Package Size and Costs



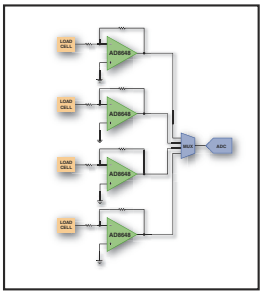
AD8334	$14.49
AD9228	$23.50
AD9219	$15.98

www.analog.com/ednc urrents

High channel count systems typically require a significant number of amplifiers to enable the ultrasound AFE to render an accurate, high quality image. The AD8334 quad VGA sets a high standard of performance by achieving a 101 dB SNR (BW = 5 MHz). In addition to superior image quality, the AD8334 uses 20% less area per channel, reduces per-channel power consumption by 20%, and cuts per-channel costs by 10% compared to other devices. On-chip overload protection shields the AD8334 from near-field ultrasound signals, and a user-selected clamping level prevents input overload to a subsequent ADC. The AD8334 also features an input noise voltage level of only 0.74 nV/$\sqrt{\text{Hz}}$, while overload protection shields the device from ultrasound near-field signals, and a selectable output clamping feature allows the VGA to protect the ADCs from signal saturation.

The AD8334, coupled with the 12-bit AD9228 or 10-bit AD9219 quad ADC, provides a complete optimized analog front end (AFE).

Versatile 24 MHz Quad CMOS Amp Offers High Performance Value

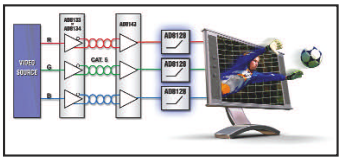


AD8648	$1.10

www.analog.com/ednc urrents

The AD8648 is a quad, low voltage, rail-to-rail input/output amplifier ideal for a variety of dynamic sensing and control applications including ATE sensors, shunt circuits, photodiode circuits, and process control. The combination of 24 MHz bandwidth, low noise of 8 nV/$\sqrt{\text{Hz}}$ (1 kHz), 1 pA input bias current, a slew rate of 12 V/μs, and a high drive current of 150 mA. The AD8648 operates from 2.7 V to 5 V and is specified from –40°C to +125°C.

Video Receiver Compensates for Category-5 Cable Losses



AD8128/AD8133/ AD8134/AD8143	$2.59

www.analog.com/ednc urrents

The AD8128 is a high speed, differential receiver/equalizer that compensates for the transmission losses of unshielded twisted pair (UTP) Category-5 (Cat-5/Cat-5e) cables. An equalized bandwidth of 120 MHz can be achieved for 100 meters of cable. The AD8128 can be used as a standalone receiver/equalizer, or in conjunction with the AD8143, triple differential receiver. Used in combination with a triple differential driver such as the AD8133 or AD8134, the AD8143 and AD8128 offer a complete low cost solution for sending and receiving red-green-blue (RGB) video signals over UTP cable.

HDMI/Analog Dual Display Interface for LCD TVs, Projectors, PDP TVs, and Other Advanced TV Applications

AD9880KSTZ-100 (100 MHz version)	$7.94
AD9880KSTZ-150 (150 MHz version)	$9.19

www.analog.com/ednc urrents

The AD9880 offers designers the flexibility of an analog interface and high definition multimedia interface (HDMI) receiver integrated on a single chip. Also included is support for high bandwidth digital content protection (HDCP). The AD9880 is a complete 8-bit, 150 MSPS monolithic analog interface, optimized for capturing component video (YPbPr) and RGB graphics signals. Its 150 MSPS encode rate capability and full power analog bandwidth of 300 MHz supports all HDTV formats (up to 1080p) and FPD resolutions up to SXGA (1280 × 1024 at 75 Hz). The analog interface includes a 150 MHz triple ADC with internal 1.25 V reference, a phase-locked loop (PLL), and programmable gain, offset, and clamp control. The user provides only 1.8 V and 3.3 V power supply, analog input, and Hsync. The AD9880's on-chip PLL generates a pixel clock from Hsync. The digital interface contains a HDMI v1.1 compatible receiver to receive encrypted video content, and it supports all HDTV formats (up to 1080p) and display resolutions up to SXGA (1280 × 1024 at 75 Hz). Fabricated in an advanced CMOS process, the AD9880 is provided in a space-saving 100-lead LQFP surface-mount Pb-free plastic package and is specified over the 0°C to 70°C temperature range.

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New Capacitance-to-Digital Converter Uses Advanced Sensing Technology to Improve Accuracy and Reliability of Touch Controls in Hand-Held Consumer Electronics

Available in high volume production for $1.09 (more than 1k).

www.analog.com/edncurrents

Analog Devices introduces a fully programmable, high performance capacitance-to-digital converter (CDC) to meet the most challenging aspects of developing a capacitive touch-screen interface. The AD7142 has been specifically designed for capacitance sensor applications, resulting in a high performance, low power, easy to implement solution. The programmable features provide the interface designer with added flexibility when developing capacitive sensor PCB or flex circuits, without the requirement to include RC tuning components to compensate for PCB and flex circuit parasitic capacitances. In addition, the AD7142 on-chip environmental and adaptive threshold sensitivity processing algorithms have been carefully chosen to produce a fully reliable capacitive sensor interface over changing environmental and user type conditions, making it ideal for mobile environments. The AD7142 Evaluation Board is available now for $199.00 through the ADI Sales office.

Drive High Speed ADCs with the Lowest Distortion Ever

AD8352 $3.49

www.analog.com/edncurrents

Presenting the lowest distortion and the highest linearity differential amplifier designed to drive 12-bit to 16-bit ADCs at the highest practical intermediate frequencies (IF). The AD8352 is designed to drive 12-bit to 16-bit ADCs at the highest practical intermediate frequencies used within next generation 3G and 4G cellular and broadband WiMAX wireless infrastructure equipment. The AD8352 is capable of maintaining exceptional performance when driving high speed ADCs up to 380 MHz, far exceeding the 100 MHz achieved by competing diff amps. The AD8352 simplifies design complexity, allowing the user to select the desired gain from 0 dB to 24 dB with one external resistor. With the ultralow distortion specs (82 dBc HD3 at 180 MHz), and 41 dBm OIP3 packaged in a space-saving 3 mm × 3 mm LFCSP package, drawing a mere 37 mA, the AD8352 is the ideal choice for driving high speed, high performance ADCs.

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BY MICHAEL FURLONG AND ALI GHIASI • BROADCOM CORP

Electronic dispersion compensation brings native 10 Gbps to networks

AT 10 GBPS, DISPERSION HAS A DOMINANT EFFECT ON OPTICAL-LINK PERFORMANCE FOR LONG- AND SHORT-HAUL-NETWORKING APPLICATIONS. TO HANDLE THIS DISPERSION, DEVELOPERS MUST EITHER UPGRADE THE FIBER INFRASTRUCTURE OR IMPLEMENT DISPERSION COMPENSATION.

Bringing new efficiencies to high-speed-optical-communications applications continues to challenge scientists and engineers alike. Whenever they overcome the current set of challenges, the demand for higher bandwidth over greater distances pushes the limitations of technology. Effects that designers previously ignored because they were below the noise floor at lower data rates and distances suddenly become significant design barriers.

Today, 10-Gbps, long-haul, and metropolitan SONET (synchronous-optical-network) OC (Optical Carrier)-192 optical links over SMF (single-mode fiber) can reach only to approximately 80 km, primarily because of impairments in the fiber. Similar problems arise in data-center and backbone applications in which 10-Gbps Ethernet links operating over legacy OM1 (optical-module) MMF (multimode fiber) can reach no more than 26m because of the effects of signal dispersion at these higher data rates. What was acceptable noise at 1 and 2.488 Gbps is debilitating at native 10 Gbps.

IT managers and carriers need to be able to cost-effectively scale networks using the infrastructure. At OC-48 and 1-Gbps rates, links can operate beyond 80 km and 26m distances with little dispersion and without significant signal-integrity impact. At 10 Gbps, however, dispersion has a dominant effect on optical-link performance for most long- and short-haul-networking applications. To handle this dispersion, developers must either upgrade the fiber infrastructure or implement some form of dispersion compensation.

Currently, both the OIF (Optical Internetworking Forum) and the IEEE have taken on the challenge of increasing the reach and reliability of 10-Gbps technology. They will address dispersion for both long- and short-haul applications with EDC (electronic-dispersion-compensation) technology to account for optical dispersion in the electrical domain. Through the use of these standards, designers can consistently apply EDC throughout networks, enabling carriers and IT managers to cost-effectively and reliably upgrade their networks.

In collaboration with the ITU (International Telecommunications Union), the OIF is defining the SMF EDC Standard under the ITU-TSG15. The standard defines long-reach, 10-Gbps, OC-192 SONET links operating over 145-km distances or 120 km with worst-case fiber. It enables seamless upgrades from OC-48 without the need to replace fiber or deploy expensive and bulky DCF (dispersion-compensated fiber). The organizations intend that the standard will address longer reach applications in which the minimum chromatic dispersion must be at least 2400 psec/nm.

For short-reach applications, the IEEE is developing the 802.3aq standard for upgrading 1-Gbps links to 10 Gbps over MMF. Most applications now run 1-Gbps links, and a few 10-Gbps deployments use parallel formats of 10G-BaseLX (local-exchange) 4 PMD (polarization-mode dispersion)—that is, four 2.5-Gbps links over OM1 fiber at distances to 300m. The 802.3aq standard will run serial 10-Gbps links over legacy OM1 MMF at distances to 220m.

Beyond bandwidth and distance considerations, the market factors driving the development and deployment of these two standards include legacy-fiber upgrades, lower costs, and increased overall link reliability. In the case of long-reach ITU-TSG15, carriers will be able to replace transponder modules, along with appropriate back-end components, such as framers, with 10-Gbps transponders. As a result, they will be able to upgrade equipment without upgrading the fiber.

One of the primary attractions of short-reach 802.3aq is that

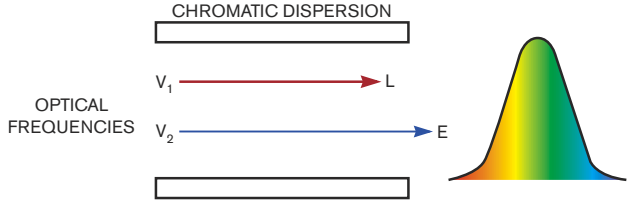

Figure 1 Because each light wavelength comprises different colors, the greater the distance light travels, the wider the pulse of light that spreads. Chromatic dispersion results in adjacent pulses that interfere with each other, leading to intersymbol interference.

carriers can run 10-Gbps links in a native serial format using a less complicated module than LX4. LX4 modules use four wavelength-stable lasers and a complex optical multiplexer, which increase overall system cost and require detailed integration and testing. In comparison, 802.3aq modules require only one wavelength of light. As a result, they consume less power, are easier to maintain and are thus more reliable, and are approximately one-half the cost of 10GBaseLX4 PMD links. Additionally, manufacturers promise even lower cost and smaller modules that they will base on the XFP (10-Gbps small-form-factor pluggable module).

LX4 PMD links are also more reliable than current links. Manufacturers are now developing or shipping products employing these standards, effectively compensating for known sources of interference and effecting substantial improvements in signal quality and therefore overall link reliability (**Table 1**).

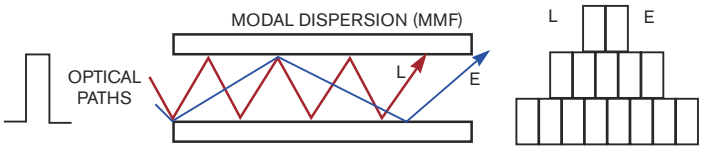

Figure 2 Imperfections in fiber and continued degradation over time cause modes to propagate through the fiber at different speeds. This situation leads to dispersion and potential overlapping of light.

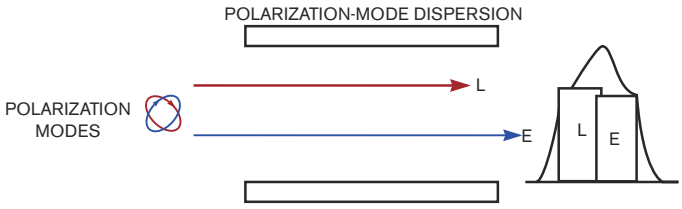

Figure 3 PMD causes a single pulse to spread at the far end because of the delayed arrival of the two perpendicular polarization modes within the fiber.

SOURCES OF DISPERSION

EDC addresses three main types of interference that lead to link impairment at 10-Gbps rates: chromatic dispersion, modal dispersion, and PMD. These types of interference depend on the symbol rate—that is, as signal speeds increase, dispersion has a greater effect. Hence, these types of dispersion have taken center stage in the migration to 10-Gbps networks.

Chromatic dispersion, the result of physical and waveguide properties, manifests itself as the spreading of a pulse of light as it travels over great distances. Optical lasers output pulses of light with a finite spectrum comprising colors. The longer the fiber over which the pulse travels, the wider the pulse spreads out (**Figure 1**). Difficulties arise when the resulting energy from a pulse begins to interfere with that of an adjacent pulse. This interference causes ISI (intersymbol interference) in the electrical domain. The spreading of symbols across each other causes errors; the receiver side of the link cannot easily distinguish the symbols because they are no longer at ideal levels. Depending on the fiber, pulse spreading may cross several UIs (unit intervals); a dispersion of one UI means that adjacent symbols within the same symbol string begin to interfere with each other.

SMFs typically have a dispersion slope of about 17 psec/nm at 1550 nm, or approximately the operating range of a long-haul transmission system. Manufacturers quantify chromatic dispersion by the distance light travels along the fiber. A pulse with a center frequency of 1550 nm transmitting over 140 km would experience a total chromatic dispersion of approximately 2400 psec/nm, which is equal to the specification for the OIF's upcoming ITU SMF long-reach standard.

Interference between modes of light arriving at a receiver at different times causes modal dispersion. As a result, modal dispersion is specific to MMF in short-reach data centers and backbones. Modal dispersion arises from imperfections in fiber that progressively degrade light, causing the light to spread, disperse, and eventually overlap (**Figure 2**).

PMD, typically a concern of SMF applications, is a phenomenon in which a single pulse appears as multiple pulses farther down the fiber (**Figure 3**). Optical fiber supports two perpendicular polarization planes, and ideal fiber would transport both polarization signals to arrive at the receiver side at the same time, appearing as a single pulse. However, fiber is neither perfectly round nor stress-free, which leads to phase shifting of the pulse. Designers can compensate for PMD using standard receivers for applications requiring reaches of less than 80 km. As link distances increase, however, the effects of PMD are statistical and complex to measure. If compression or kinks have damaged the fiber, for example, performance degrades appreciably more quickly; consider that a single kink could cause two components of light to travel at 90° to each other. For this reason, the condition of the fiber can have a more pronounced effect on signal integrity than the length of the link.

COMPENSATION OPTIONS

You can effectively implement EDC using a variety of equalization algorithms. The three most common are CTFs (continuous-time filters), FFE/DFE (feedforward-equalizer/decision-feedback-equalizer)-algorithm combinations, and sophisticated MLSE (maximum-likelihood-sequence-estimator) equalization. CTFs offer the simplest, most cost-effective, and lowest power EDC implementation. By boosting or bandlimiting the signal within the frequency band of interest, a CTF can adjust the analog bandwidth of the optical front end, effectively acting as a lowpass filter. By amplifying certain frequencies and attenuating others through waveshaping, a CTF can compensate for chromatic dispersion. However, you can reduce high-frequency noise only so much before the CTF begins to filter the signal, as well, severely curtailing such compensation. Thus,

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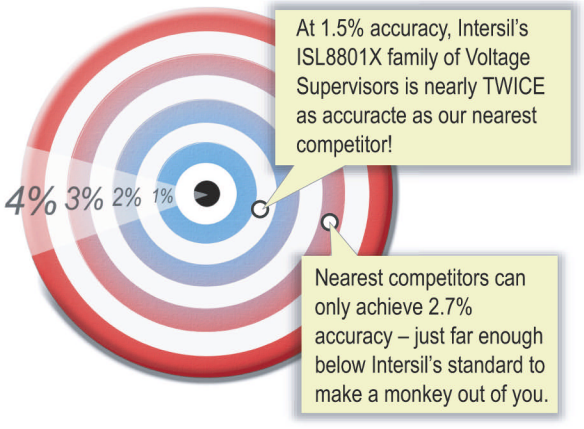
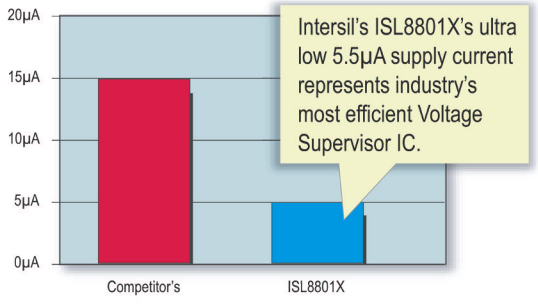


Comparative Power Consumption



ISL8801X Family's Available Features and Functions	ISL88011	ISL88012	ISL88013	ISL88014	ISL88015
Active-Low Rest ($\overline{RST}$)	●	●	●	●	●
Active-High Rest (RST)	●	●	●		
Watchdog Timer (WDI)			●		●
Dual Voltage Supervision		●			
Adjustable POR Timeout (C_{POR})	●			●	
Manual Reset Input ($\overline{MR}$)	●	●	●	●	●
Fixed Trip Point Voltage	●	●	●		
Adjustable Trip Point Voltage		●		●	●

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CTFs are appropriate only in applications in which dispersion is not excessive.

FFE/DFE algorithms apply a more sophisticated approach to compensation than that of a CTF. FFE/DFE implementations use multitap algorithms to compensate for ISI that exceeds one UI of interference. An EDC implementation comprises an AGC (automatic-gain-control) block, a CTF/FFE block, a DFE block, a CDR (clock- and data-recovery) block, and an LMS (least-mean-squared) adaptation block (**Figure 4**).

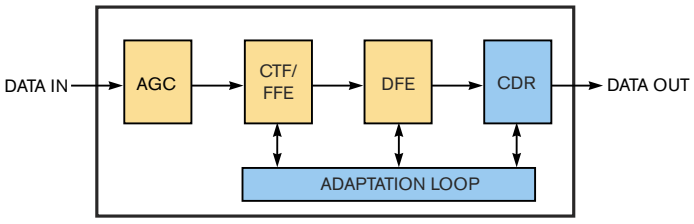


Figure 4 An EDC implementation comprises an AGC block, a CTF/FFE block, a DFE block, a CDR block, and an LMS (least-mean-squared) adaptation block.

When there is only a single UI of interference, compensation involves determining whether an adjacent symbol has spread into the current symbol and then adding or subtracting the symbol. When more than one UI of interference is present, a symbol can spread and distort several adjacent symbols, making compensation more complex. FFE removes distortion before a symbol's primary energy point or precursor area. DFE compensates for interference following a symbol's primary energy point or postcursor area.

MLSE implementations provide even more sophisticated equalization architectures. Incorporating Viterbi-decoder algorithms, an MLSE requires a DSP approach to filtering. Although an MLSE can achieve better performance than an FFE/DFE, DSP implementations are generally more complex and often consume two to four times the power. For these reasons, MLSE-based approaches most often find use in applications having little room for compromise in performance. For example, MLSE compensates for severe nonlinearity in fiber or in ultra-long-haul applications.

The most common EDC implementation uses a combination of FFE and DFE, providing a higher level of performance and reliability than do CTFs but at a more reasonable power cost than MLSE implementations require. In addition, an analog FFE/DFE design typically has lower power dissipation than a digital implementation because there is no need to convert the analog signal into the digital domain using high-speed ADC or DSPs. Typically, designers base an FFE implementation on an analog distributed amplifier using various on-chip transmission lines to create delay elements. The DFE portion uses sample data to determine signal quality and requires a bit-rate clock, so you can implement it primarily in analog or primarily in digital, depending on your application's architecture.

Power consumption is only one consideration, however. You must also consider performance stability over extreme operating conditions, as well as other issues. For example, model dispersion in MMF is often more of a factor than it is in SMF. As a consequence, equalization for short-reach MMF is often more sophisticated than that for long-haul SMF. EDC also has a substantial effect on signal reliability. Traditional receivers without EDC can recover an optical signal only if the dispersion is less than approximately one-half UI over the length of the fiber. The new IEEE 10-Gbps standard, however, supports runs as long as 220m using OM1-type 62.5-micron fiber and specifies that the receiver must be able to handle more than four UI of dispersion. Without EDC, you cannot possibly meet this requirement.

DYNAMIC EDC

Adaptability is an essential characteristic for any successful network. Every optical link has characteristics that its length, quality, condition, and other important factors determine. Equipment needs to automatically adapt to a link when the user installs it to achieve the best performance, efficiency, and reliability. Additionally, as fiber degrades over time and introduces new sources of interference, such as new kinks in the fiber, line cards must refine compensation algorithms to adapt to these changes. In this way, designers can achieve further cost savings by eliminating the need for hand-tuning links for reach and wavelength. Rather, with self-adaptable EDC-enabled equipment, users can install line cards without manual tuning for true plug-and-play deployment. An adaptive EDC implementation can improve more than just reliability. Because designers can tailor equalization for an application, adaptive EDC also facilitates the use of a single-board design across multiple applications.

Self-adaptation requires closed-loop-feedback mechanisms that enable equipment to calibrate itself by slightly modifying filters and gains that improve signal response until the system achieves an ideal signal. Using well-established LMS algorithms to implement EDC, you can easily implement efficient self-adaptation. Many silicon vendors are looking to integrate EDC directly on transceivers to further simplify this process for developers.

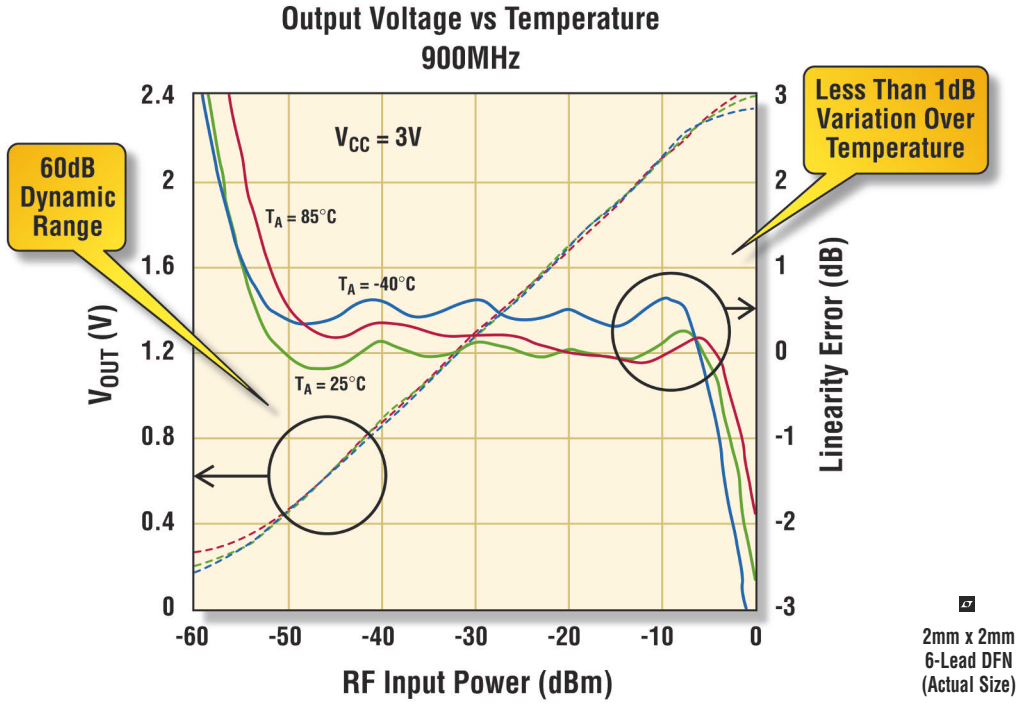
Clearly, 10-Gbps Ethernet is an important enabling technology in

TABLE 1 SIGNAL QUALITY WITH AND WITHOUT EDC

Technology	10-Gbps Ethernet short reach	10-Gbps Ethernet short reach, with EDC	10-Gbps SONET long haul	10-Gbps SONET long haul, with EDC
Standard	802.3ae	802.3aq	G.959.1	G.959.1
Wavelength (nm)	850	1300	1550	1550
Fiber (microns)	MMF (62.5/125)	MMF (62.5/125)	SMF (9)	SMF (9)
Maximum distance	26m	220m	80 km	145 km
Dispersion	NA	NA	1600 psec/nm	2400 psec/nm
Bit-error rate (Hz)*	1×10^{-12}	1×10^{-12}	1×10^{-12}	1×10^{-12}
Path penalty*	NA	NA	2 dB	2 dB*

***Without EDC, the path penalty would be more than 10 dB, and bit-error rate would be less than 1×10^{-6}.**

Temperature Stable 60dB RF Log Detector



2mm x 2mm
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Features

- Exceptional Stability Over Temperature
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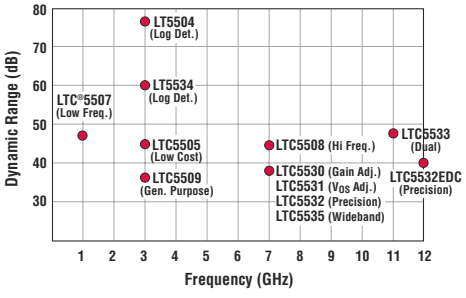
- Tiny 2mm x 2mm DFN Package
- Wide Bandwidth Operation from 50MHz to 3GHz
- 2.7V to 5.25V Supply
- 38ns Full-Scale Settling Time

Broad RF Detector Coverage



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data-center, storage-network, and back-haul applications. Current 10-Gbps implementations have aggregated only four 2.5-Gbps links because of the effects of signal dispersion at native 10 Gbps. With the means to compensate for dispersion at high signal frequencies, IT managers and carriers will be able to cost-effectively upgrade 1-Gbps and OC-48 links to native 10 Gbps, all without laying new fiber or deploying bulky DCFs.

EDC is an effective means of compensating for dispersion and does so across the optical spectrum from short- to long-haul applications. By compensating for optical dispersion in the electrical domain, EDC enables developers to upgrade network links without changing optical components. It also significantly increases overall reliability and the distance that links can run.

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EDC is an essential ingredient for the successful deployment of native 10-Gbps links. Both the OIF and the IEEE recognize this fact and have been managing the development of EDC to ensure that it stabilizes, rather than—lacking an industry standard—impedes, the 10-Gbps-Ethernet market. As expected, the OIF's ITU-TSG15 is nearing ratification. Interoperability testing between industry leaders is under way, and the organization should approve the standard with no fundamental changes. Likewise, the IEEE's 802.3aq standard is making significant headway. Currently in draft status, the standard should achieve ratification by midyear. In the meantime, developers can continue to design 10-Gbps equipment knowing that they can achieve the performance, distance, cost, and reliability expectations of the market. EDN

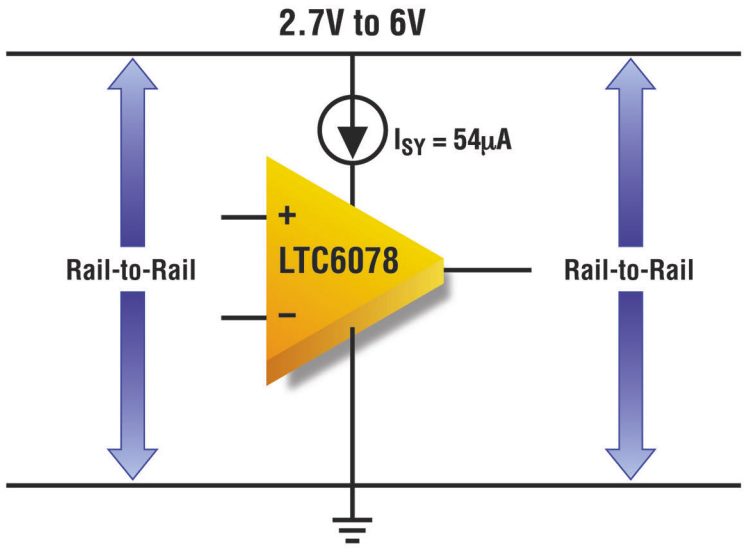
AUTHORS' BIOGRAPHIES

Michael Furlong is a senior product-line manager with Broadcom Corp. He manages the business and strategic direction of the company's high-speed-interconnect-product line. He received a bachelor's degree in electrical engineering and a master's in business administration from the Florida Institute of Technology (Melbourne).

Ali Ghiasi, PhD, is the chief architect for Broadcom Corp's optical business. His current interests include EDC (electronic-dispersion-compensation) applications for datacom and telecom, storage networking, and next-generation optical interfaces, and he is a founder of the XFP (10-Gbps small-form-factor pluggable module) MSA (multisource agreement). Ghiasi has a doctorate in electrical engineering from the University of Minnesota (Twin Cities) and master's and bachelor's degrees from North Dakota State University (Fargo). Ghiasi has written for more than 50 publications, as well as architectural proposals for the standards bodies IEEE, OIF, FC, and InfiniBand. In addition, he is the named inventor on more than a dozen patents and patent applications in high-speed communications and interconnects.

True Precision CMOS Op Amp

V_{OS} = 25µV Max.
T_CV_{OS} = 0.7µV/°C Max.
I_B = 1pA Max.



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- Packages: Dual in MSOP and DFN
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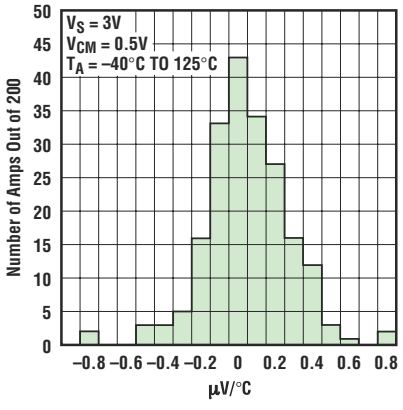
V_{OS} Drift Distribution



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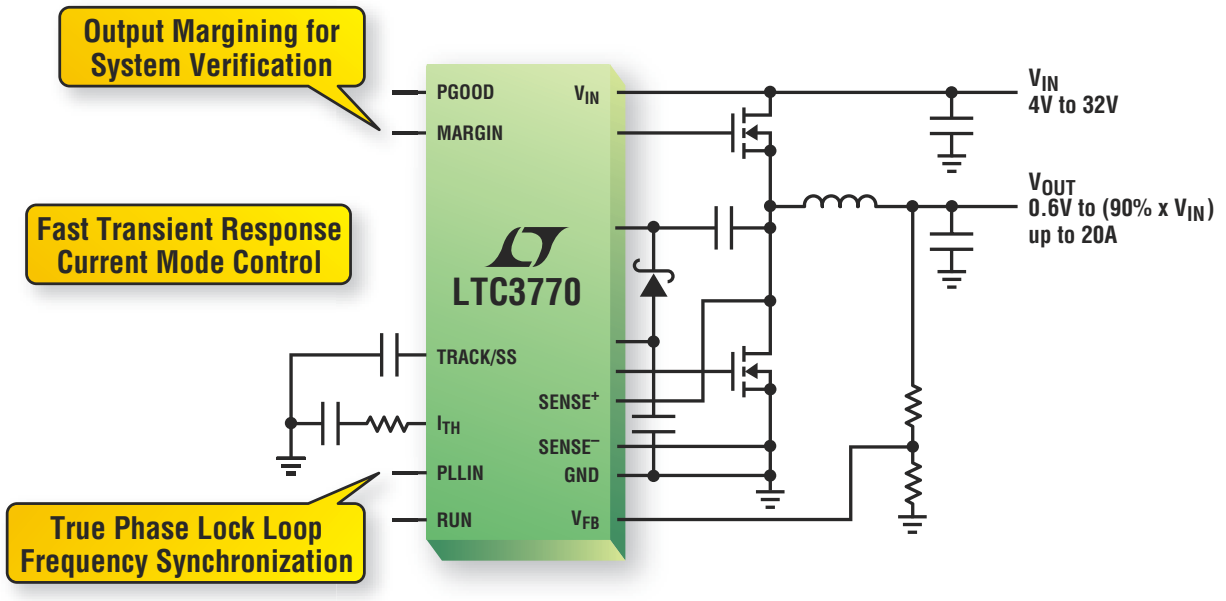
Accurate and Fast



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- $T_{ON(MIN)} \leq 100ns$
- Adjustable Switching Frequency
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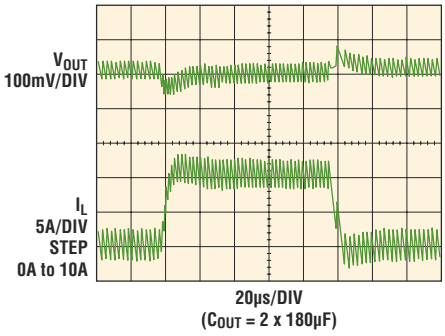
Fast Transient Response



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DESIGN NOTES

10A High Performance Point-of-Load DC/DC µModule

4.5V to 28V Input, 0.6V to 5V Output in a 15mm × 15mm × 2.8mm Package

Design Note 385

Eddie Beville

Introduction

Advancements in board assembly, PCB layout and digital IC integration have produced a new generation of densely populated, high performance systems. The board-mounted point-of-load (POL) DC/DC power supplies in these systems are subject to the same demanding size, high power and performance requirements as other subsystems, making it difficult to meet the rigorous new POL demands with traditional controller or regulator ICs, or power modules.

For such demanding applications, an ideal POL power supply must meet high performance specifications while simplifying board assembly—mounting similar to other surface mount ICs on the board without requiring special tooling. Such POL DC/DC regulators must also demonstrate exceptional thermal performance with innovative packaging technology. Power density increases without the danger of overheating and shortened device life. The LTM®4600 µModule™ does all of these things.

10A DC/DC µModule in IC Form Factor

The LTM4600 µModule is a complete power supply point-of-load DC/DC regulator with a low profile IC form-factor. The controller, onboard inductor, MOSFETs and compensation circuitry are all housed in a 15mm × 15mm × 2.8mm LGA surface mount package which weighs only 1.73g (Figure 1). These size parameters allow the LTM4600 to be mounted on the back side of a system board, taking advantage of the otherwise unused space. The µModule switches at a nominal 800kHz in a synchronous topology to offer very high efficiency in a small form factor and low profile.

The µModule is offered in two versions. The LTM4600EV operates from an input supply range of 4.5V to 20V; the LTM4600HVEV operates from 4.5V to 28V. Both offer adjustable output voltages from 0.6V to 5V and output currents of 14A peak and 10A continuous. Fault protection features include overvoltage protection and overcurrent protection.

Quick and Easy Design

Figure 2 shows a typical LTM4600EV design for a 2.5V output and Figure 3 shows the efficiency of the circuit. Although bulk capacitors on the input and output suffice in most applications, this design uses two low ESR 10µF 25V ceramic capacitors to reduce input RMS ripple. The output voltage is set with an external resistor from the VOSET pin to ground. The output capacitors are selected for low ESR to maintain an initial voltage droop of the output voltage to approximately $\Delta V_{OUT} = I_{LOADSTEP} \bullet R_{ESR}$ in a transient step.

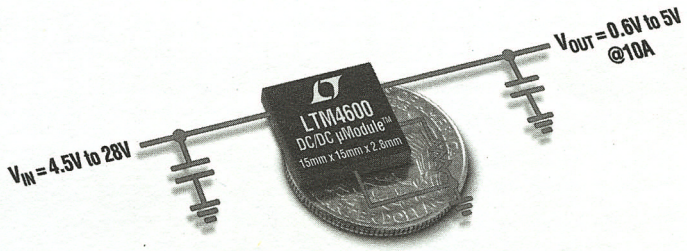
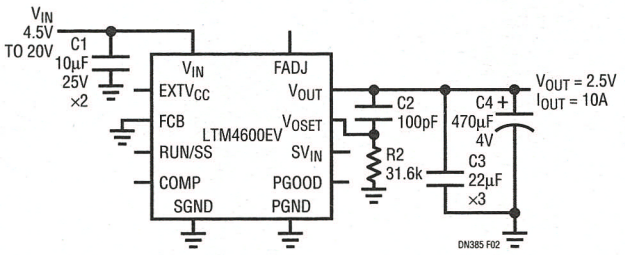


Figure 1. The LTM4600 Offers Unprecedented Power Density in a Small Package



C1: TDK C3216X5R1E106MT
C2: TDK C1005COG1H101K
C3: TAIYO YUDEN JMK316BJ226ML-T501
C4: SANYO POS CAP 4TPE470MCL

Figure 2. Few Components Are Required in this 2.5V/10A Application

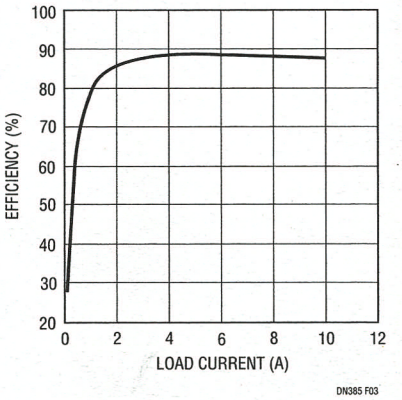


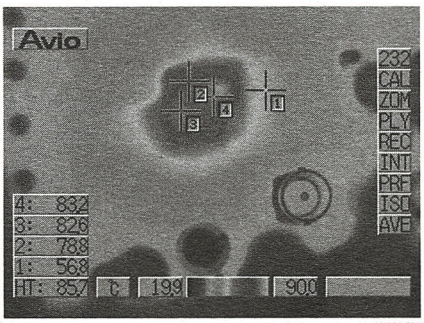
Figure 3. Efficiency of the Application in Figure 2

Thermally Enhanced Packaging

The µModule packaging has extremely low thermal resistance of 6°C/W and 15°C/W junction-to-case and junction-to-ambient, respectively. It allows heat-sinking from both the top and bottom of the device. Figure 4 shows the top view thermal imaging of the LTM4600 at full throttle with no airflow and heat sink. Refer to Application Note 103 for detailed thermal analysis and measurements.

Fast Transient Response

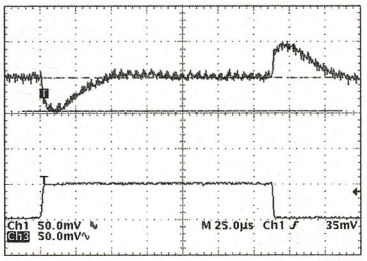
A unique feature of the LTM4600 is its no-clock-latency valley current mode architecture. This feature allows very fast loop response to rapid load transients with minimum output capacitance. Typically, the output voltage turns around in 4 to 6 microseconds and fully recovers in 20 to



CONDITIONS: 25°C, NO AIR FLOW,
NO HEATSINK, NO $EXTV_{CC}$

Figure 4. The LTM4600 Exhibits Impressive Thermal Performance, Even Without Air Flow and Heat Sink (24V to 3.3V at 10A, Top View). For a Color Representation, Download the .pdf at www.linear.com

25 microseconds. Figure 5 shows the transient deviation of only 55mV on a 2.5V output with a 5A load step. The 6µs of turnaround is acheived with only a 470µF POS cap and the three 22µF ceramics.



2.5V AT 5A/µs LOAD STEP
C_{OUT} = 3 • 22µF 6.3V CERAMICS
470µF 4V SANYO POS CAP
C3 = 100pF

Figure 5. Load Transient Response for the Application in Figure 2

Paralleling the µModule for 20A Output

The LTM4600 µModule can be used two in parallel to double the output current. The current mode architecture and precision current limiting allow two modules to equally share the output current, thus maximizing efficiency and equally distributing the heat.

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On/off buffer switches analog or digital signals

Liviu Pascu, Kepco, Flushing, NY

Many applications require a method of switching an analog or a digital signal on or off under digital control. A "wish list" of specifications for such a switch might include attenuation of less than 90 dB when the switch is in its off-state, distortion of no more than 0.002% when the switch is in its on-state, and the ability to respond to an on or an off command in 10 µsec or less. In addition, the circuit should accommodate positive- or negative-going signals, and no turn-on or turn-off overshoot should occur for either signal polarity. The list might also require that the circuit's control input must accept digital signals from most logic families and that the circuit's SNR should exceed 90 dB.

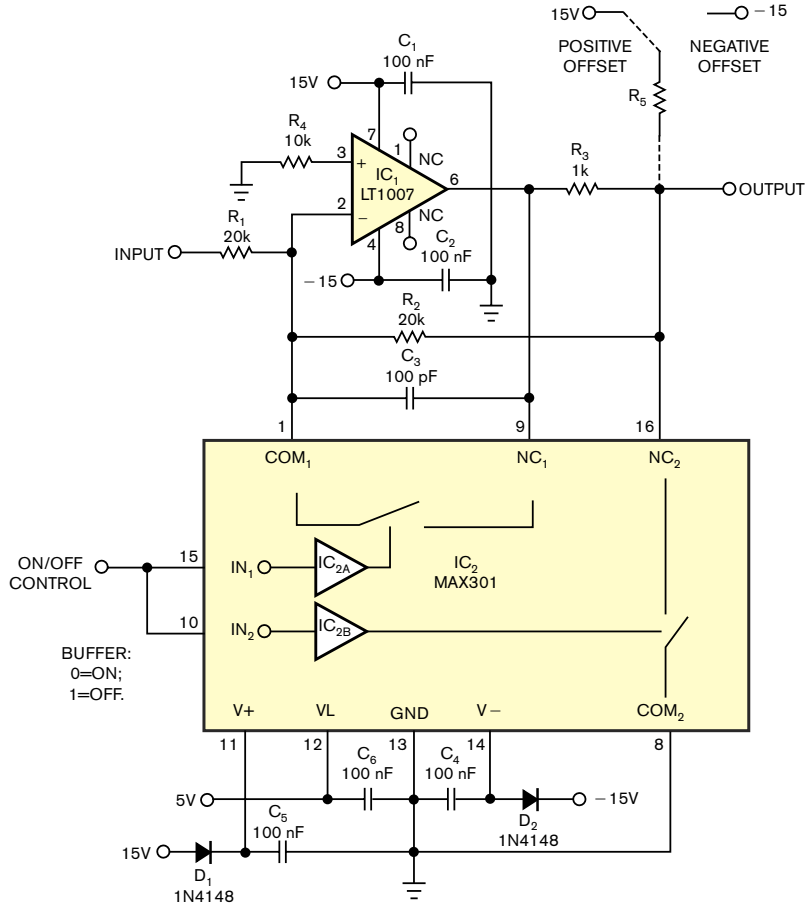

Figure 1 This buffered switch can accommodate either analog or digital signals.

The circuit in **Figure 1,** comprising IC_1, a low-noise, high-speed, precision Linear Technology LT1007 operational amplifier and IC_2, a Maxim MAX301 dual SPST, normally open analog switch, fulfills these requirements. In the circuit, V_{IN} is the input voltage, and V_{OS} and I_{OS} represent operational amplifier IC_1's voltage and current offsets of either polarity. I_{OFF} represents the off-state leakage current of either section of analog switch IC_2. In the buffer circuit, $R=R_1=R_2$, and $R_4=R/2$. Hence, $\Delta R=(R_1\times R_2)/(R_1+R_2)-R_4$.

If all resistors were identical in value, ΔR would equal zero. However, each resistor exhibits its own tolerance error, and the equation for ΔR expands to:

$$\Delta R = \frac{(R_1(1+e_1))\times((R_2)(1+e_2))}{(R_1(1+e_1))+((R_2)(1+e_2))} - \left(R_4(1+e_4)\right),$$

where e_1 through e_4 are maximum tolerance errors of ±1%. Worst-case values for ΔR occur when the tolerance values e_1 and e_2 for R_1 and R_2 are of the same sign and e_4 for R_4 has the opposite sign:

DIs Inside

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$$\Delta R = \pm\left[\frac{R(1+|e|)}{2} - \frac{R(1-|e|)}{2}\right].$$

Simplifying further, $\Delta R = \pm R\,|e|\} = \pm\{(0.01)R\}$ when you use 1%-tolerance resistors for R_1, R_2, and R_4. The combination of the resistors' tolerances with the operational amplifier's internal errors and leakage effects from switches IC_{2A} and IC_{2B} determines the buffer's accuracy. When the circuit is on, both IC_{2A} and IC_{2B} are open. The following **equation** defines the circuit's output voltage:

$$V_{OUT(ON)} = -\left\{\left[\frac{V_{IN} - V_{OS} - (I_{OS} \times \Delta R)}{R_1}\right]\right\} - (I_{OFF}) \times R_2.$$

Simplifying further, you can calculate $V_{OUT(ON)}$ as: $V_{OUT(ON)} = -(V_{IN}) + V_{OS} + ((I_{OS}) \times (\Delta R)) + ((I_{OFF}) \times (R))$.

Most of today's solid-state switches present an I_{OFF} of less than 1 nA, and you can select an op amp for IC_1 whose V_{OS} is less than 50 µV and whose I_{OS} is less than 50 nA. Thus, for the resistor values in **Figure 1**, the maximum error for the amplifier's on-state is approximately 80 µV, or 0.0008%, when referred to a 10V nominal output. You can determine the minimum allowable value of the amplifier's load resistance by solving the following **equation**:

$$R_{LOAD} > \left(\frac{R_3}{\frac{V_{SAT}}{V_{OUT(MAX)}} - \frac{R_3}{R_2} - 1}\right),$$

where V_{SAT} represents the op amp's maximum saturated output voltage—usually, 13.5V for ±15V power-supply voltages. For example, using the resistor values in **Figure 1** and assuming a maximum output voltage of 10V, you can calculate a minimum allowable load resistance of 3.3 kΩ.

Also, I_{AMP}, the current from IC_1, should be less than the device's specified maximum current output: $I_{AMP} = (V_{OUTMAX}) \times [(1/R_2) + (1/R_{LOAD})]$.

Using these values, you can determine that I_{AMP} is 3.5 mA, which is less current than most op amps as sources deliver. When the amplifier is off, switches IC_{2A} and IC_{2B} are closed. In this state, the worst-case output occurs for V_{INMAX}. IC_1's offset errors are negligible with respect to the full-scale input voltage. Therefore, for the real case in which the on-resistance of IC_{2A} and IC_{2B} is much less than the load resistance, the following **equation** defines the circuit's output voltage: $V_{OUTOFF} = -[(V_{IN} \times R_2 \times R_{ON} \times R_{ON})/(K_1 + K_2 + K_3 - K_4)]$, where $K_1 = R_1 \times R_2 \times R_3$, $K_2 = R_1 \times R_3 \times R_{ON}$, $K_3 = R_1 \times R_{ON} \times R_{ON}$, and $K_4 = R_1 \times R_2 \times R_{ON}$. For $R_1 = R_2 = R$ and $R_{ON} << R$, and $R_{ON} << R_3$, the **equation** simplifies to: $V_{OUTOFF} = -[(V_{IN} \times R_{ON} \times R_{ON})/(R \times R_3)]$.

Many of today's analog switches present a maximum 20Ω on-resistance, and, using the resistor values in **Figure 1** and an input voltage of 10V, you can calculate that output voltage to be approximately 200 µV, or 0.002%, when referred to a 10V nominal output. Amplifier IC_1's slew rate limits the circuit's dynamic behavior, because analog switch IC_2 generally switches in much less than 1 µsec. Using an operational amplifier with a slew rate of 1.5V/µsec yields a circuit-response time of 10 µsec.

For applications that require unipolar outputs when the amplifier is in its off-state, you can add a known output-offset voltage by connecting resistor R_5 between the buffer's output and the power-supply voltage of the same polarity as the desired offset voltage. Note that IC_1's output must be able to sink current. Adding resistor R_5 doesn't affect the circuit's output voltage in its on-state because the closed-loop gain lowers the amplifier's output impedance.

To analyze the circuit's offset output voltage, assume that IC_{2A} and IC_{2B} present an on-resistance that's much less than R_{LOAD}, R_2, and R_5. The following **equations** define the circuit's positive and negative offset-output voltages, $V_{OUT(OS)}$ and $-V_{OUT(OS)}$, respectively:

$$V_{OUT(OS)} = \left[+|V_S| \times \left(\frac{R_{ON}}{R_5}\right)\right] + \left[|V_{IN}| \times \left(\frac{R_{ON}}{R_2}\right) \times \frac{R_{ON}}{R_3}\right].$$

$$-V_{OUT(OS)} = \left[-|V_S| \times \left(\frac{R_{ON}}{R_5}\right)\right] - \left[|V_{IN}| \times \left(\frac{R_{ON}}{R_2}\right) \times \frac{R_{ON}}{R_3}\right].$$

To make the offset voltage less dependent on the input signal, calculate the maximum value for R_5 as:

$$R_5 < \frac{I}{10} \times \frac{V_S}{V_{IN}} \times \frac{R_2}{R_{ON}} \times R_3.$$

Using the resistor values in **Figure 1**, solving this **equation** produces a minimum reliable offset voltage of 2 mV; the value of R_5 must be 150 kΩ or less. The maximum current-sinking ability of IC_1 determines the minimum value of R_5. EDN

Single switch serves dual duty in small, microprocessor-based system

Steve Hageman, Windsor, CA

Traditional control-system designs use separate switches to control power and various system functions, but adding a few components to a small, microprocessor-based system can combine a control function with the system's on/off switch. For example, you can design a system to display relative humidity and temperature (**Reference 1**). This small, battery-powered system requires a microprocessor-controlled on/off power switch, which you implement with a pushbutton, and a function switch to change the display from degrees Celsius to degrees Fah-

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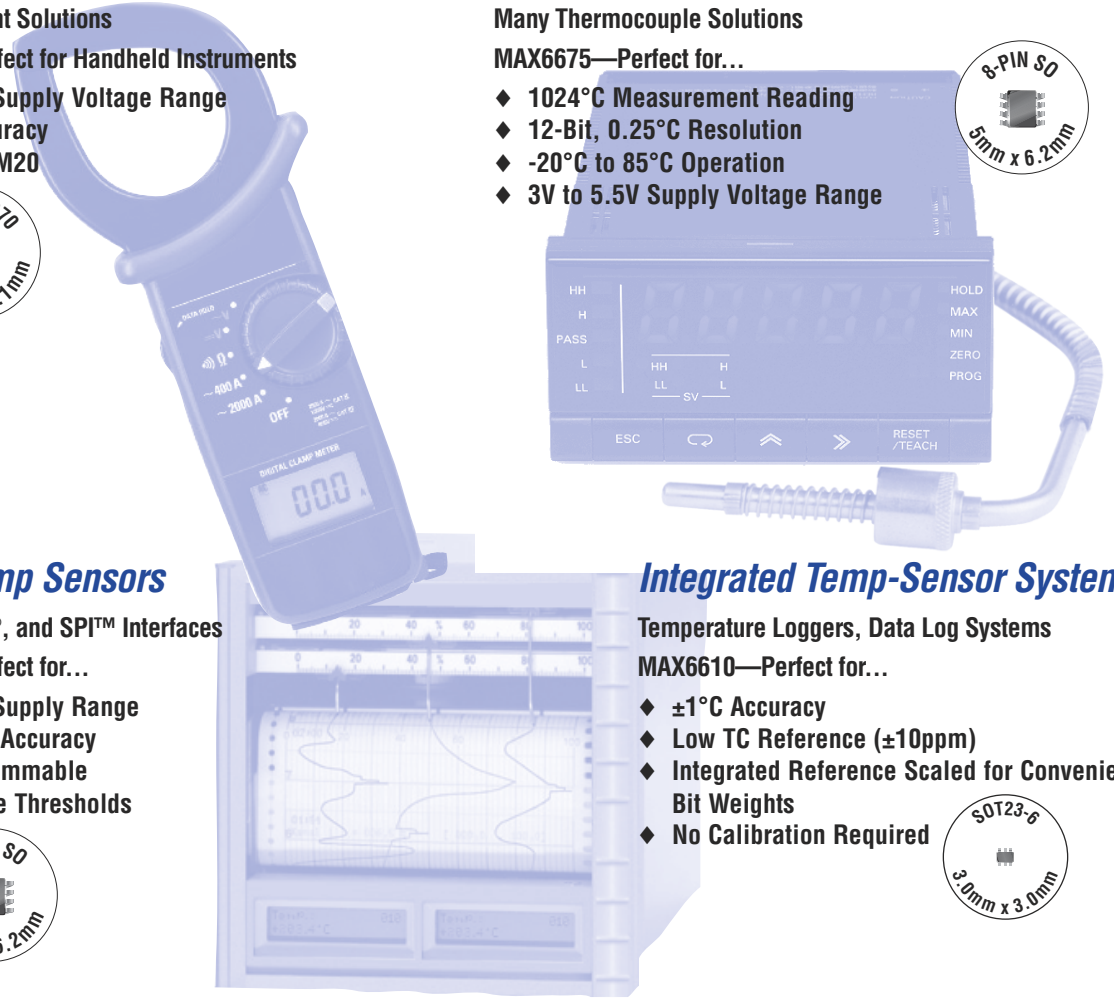

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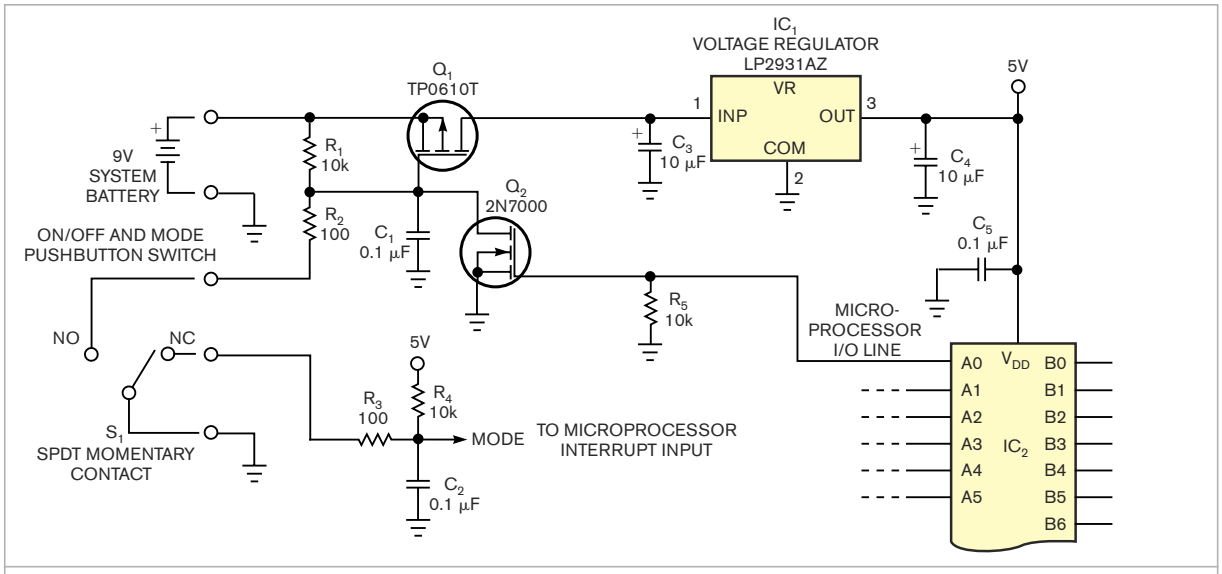

Figure 1 A single pushbutton switch can control power and select among operating modes in a simple microprocessor-based system.

renheit, which you implement as a toggle switch. From ease-of-use and total-cost perspectives, combining these two functions in a single switch makes sense.

Figure 1 shows a circuit for this application. Initially, Q_1, a P-channel MOSFET, is off because R_1 holds Q_1's gate-to-source voltage at 0V. No input reaches voltage regulator IC_1, and, thus, the system's microprocessor, IC_2, also remains off. When the operator presses the normally closed momentary-contact pushbutton switch, S_1, current flows through R_1 and R_2 to ground, developing sufficient gate-to-source voltage to turn on Q_1 and apply power to voltage regulator IC_1 and the microprocessor. Capacitor C_1 debounces the switch contact and ensures that Q_1 remains on long enough to start the microprocessor, regardless of how quickly the user presses and releases the switch. In addition, as its final task, the start-up firmware initializes the system's LCD, thus reinforcing the operator's tendency to hold the power switch in its on position long enough to ensure full start-up.

Immediately after the microprocessor powers up, it begins executing its firmware and turns on Q_2, an N-channel MOSFET, by delivering a logic one of more than 3V to Q_2's gate. In turn, Q_2 keeps Q_1 switched on, and the system runs under software control. If the operator again presses the on/off button, Q_1 remains on, and the microprocessor continues to run but pulls its mode line high. The mode line drives an interrupt input pin, and the software can use the interrupt as a toggling function or to access a wraparound, multiple-choice menu. After a suitable preprogrammed time interval, the microprocessor system turns itself off by placing a logic zero on Q_2's gate. In turn, Q_2 switches off Q_1 to remove power from the system. EDN

REFERENCE

1 Hageman, Steve, "Relative humidity/temperature meter," www.analog home.com/projects/dewpointer.html.

Isolated-FET pulse driver reduces size, power consumption

José M Espí, Rafael García-Gil, and Jaime Castelló,
Electronic Engineering Department, University of Valencia, Spain

Three-phase controlled rectifiers and inverters, matrix cycloconverters, and cascaded power stages typically comprise large numbers of power transistors, each with its own driver circuit. The circuit in **Figure 1** drives a capacitive-input power device, such as a MOSFET or an IGBT (insulated-gate bipolar transistor) with pulses of all duty cycles at frequencies of 1 to 200 kHz. A single transformer provides galvanic isolation, and the circuit consumes little power from its 15V primary-side power supply. Tested satisfactorily using several MOSFETs and IGBTs with input capacitances as high as 5 nF, the driver can accommodate higher current power transistors by resizing the driver's transistors and coupling transformer and a few passive components.

Transistors Q_1 and Q_2 transmit pulses of approximately 1-µsec duration through coupling transformer T_1 to transistors Q_3 and Q_4, which respectively charge and discharge power transistor Q_5's gate-source input capacitance. The charging pulse that Q_1 produces begins on the rising edge of the drive-control signal, and the discharge

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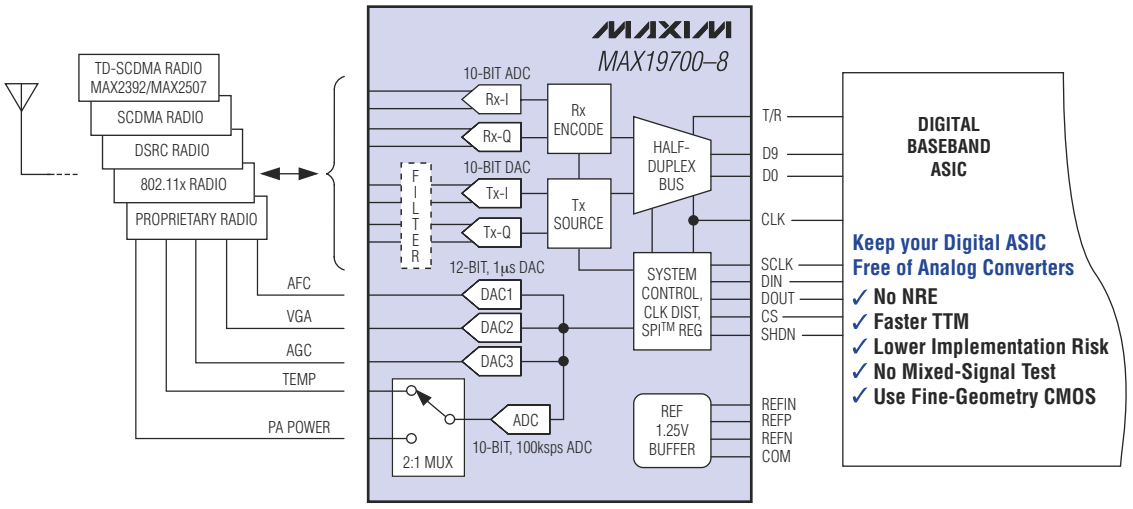

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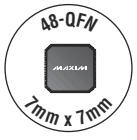

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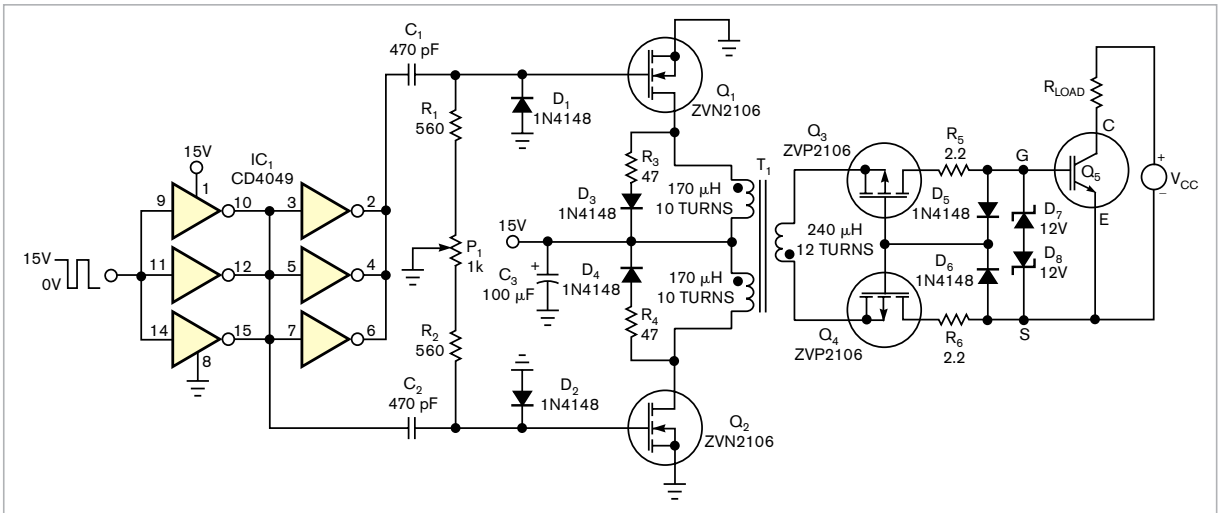

Figure 1 The isolated pulse driver transmits all duty cycles and consumes energy only during the gate charge and discharge processes.

pulse that Q_2 produces begins on the falling edge of the control signal. Differentiator circuits comprising C_1, R_1, a portion of potentiometer P_1, C_2, R_2, and the remaining portion of P_1 set the durations of the charge and discharge pulses. If necessary, adjusting P_1's setting alters the balance of the positive and negative charge and discharge voltages that Q_5's gate receives.

Transistors Q_3 and Q_4, respectively, transmit pulses to charge or discharge Q_5's input capacitance and then switch off, producing a high impedance across Q_5's input capacitance so that Q_5's gate voltage doesn't change, except for discharging slowly due to small leakage currents. Thus, the driver circuit consumes power only during the short intervals of the gate-to-source charge and discharge processes.

When transistors Q_1 through Q_4 switch off, resistor and diode pairs R_3, D_3, R_4, and D_4 form a path for transformer T_1's demagnetization current. Although they're reverse-biased most of the time, diodes D_5 and D_6 form a peak-amplitude discriminator, configured as a logical-OR circuit, to ensure that gate voltages at Q_3 and Q_4 always equal or exceed the voltage at the positive terminal of Q_5's gate-to-source capacitance.

Resistors R_5 and R_6 limit charge and discharge rates for Q_5's gate-to-source capacitance and can vary depending on Q_5's drive characteristics. Transformer T_1 comprises a Philips RM5/I core of 3E5 ferrite material with a center-

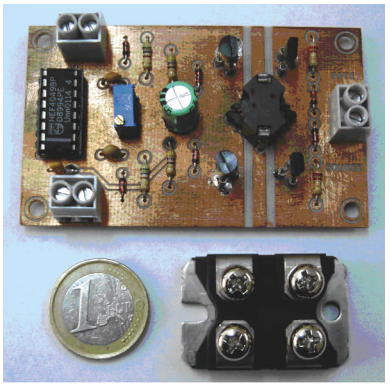

Figure 2 A top view of the isolated gate driver's prototype version shows that an isolation barrier interrupts the ground plane beneath transformer T_1 (upper right center).

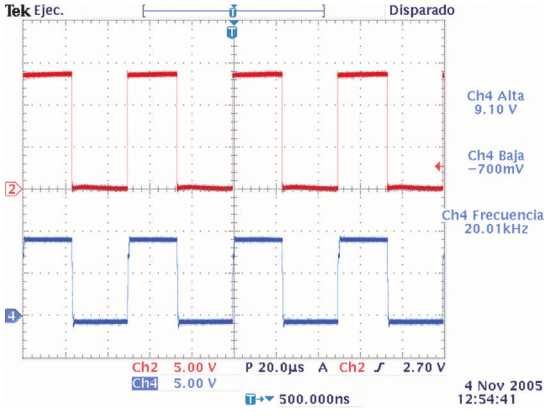

Figure 3 The top trace shows the driver-control voltage, and the bottom trace shows the gate-source voltage of an APT40GF120JRD IGBT, Q_5, at 20 kHz. You can use potentiometer P_1 to adjust the 9.1 and 20.7V high and low gate-to-source levels, respectively.

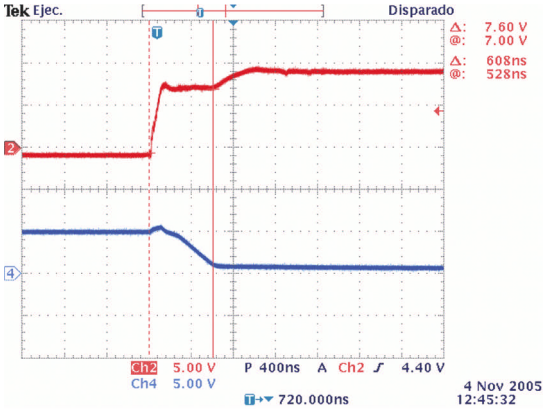

Figure 4 The top trace shows the driven transistor's gate-to-source voltage, and the bottom trace shows its collector-emitter voltage, which a probe attenuates. The transistor's load comprises a resistor that connects to a power supply.

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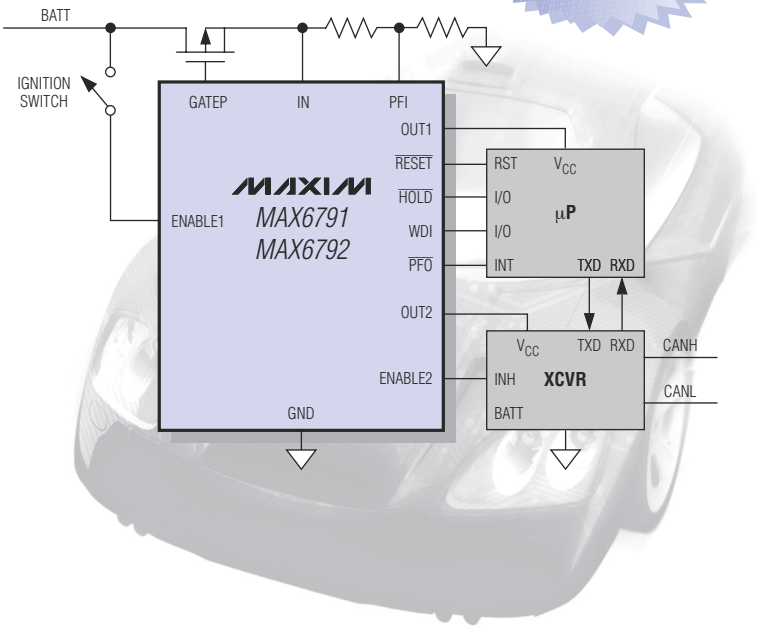

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tapped, 20-turn primary winding and a 12-turn secondary winding, both fabricated from 0.2-mm-diameter, 0.008-in, AWG #32 magnet wire.

When transistor Q_1 switches on, it induces a positive voltage in T_1's secondary winding that switches on P-channel MOSFET Q_3 and drives Q_4's internal body diode into conduction to begin charging Q_5's gate-to-source capacitance. Q_3's on-channel resistance primarily determines the charging rate. Charging ends either when the pulse terminates or when Q_5's gate-to-source voltage approximates T_1's secondary voltage minus Q_3's gate-threshold voltage.

Next, Q_3 switches off, allowing the charging current to decay to zero and the capacitance to reach its maximum positive charge. When Q_1 switches off, transformer T_1's magnetizing current resets through R_3 and D_3. The voltage at T_1's secondary winding goes slightly negative to balance the core's volt-second characteristic, which forward-biases Q_3's body diode without current, and Q_4's body diode blocks the discharge of Q_5's gate-to-source voltage.

The negative voltage you apply to Q_4's gate cannot switch on Q_4 because diode D_5's forward-voltage drop sets Q_4's gate voltage higher than the voltage at Q_5's gate. Thus, Q_5's input capacitance remains charged, and the reset path presents high impedance to this capacitance. When Q_2 switches on, the negative voltage that appears on T_1's secondary turns on Q_4 and starts the discharge process, which ends when Q_4's source-to-gate voltage equals its threshold level or when the pulse terminates. Then, Q_4 turns off, and Q_5's gate-to-source capacitance reaches its minimum negative voltage. When Q_2 turns off, T_1's magnetizing current resets through D_4 and R_4, Q_4's body diode conducts, and Q_3's body diode blocks Q_5's gate-to-source voltage. Diode D_6 applies a high voltage to Q_3's and Q_4's gates to ensure that the reset voltage at T_1's secondary doesn't drive Q_3 into conduction. Thus, all transistors remain off, and Q_5's gate-to-source capacitance remains discharged. When Q_1 next switches on, the sequence repeats.

Figure 2 shows the driver prototype compared with a €1 coin and a power transistor. The transistor, an Advanced Power Technology APT40GF-120JRD, combines an IGBT and a FRED (fast-recovery epitaxial diode) that operates at a maximum of 1200V and 60A with a gate-to-source capacitance of 4 nF. The transistor comes in a JEDEC SOT-227 package measuring approximately 1.5×1 in. (38×25 mm). **Figures 3** and **4** show experimental waveforms for the circuit of **Figure 1** to drive IGBT Q_5 at 20 kHz. The turn-on delay is approximately 600 nsec, and the total current consumption is 22 mA for a power consumption of 0.33W. When driving transistors that present a lower gate-to-source capacitance, the circuit's turn-on delay and power consumption both decrease. EDN

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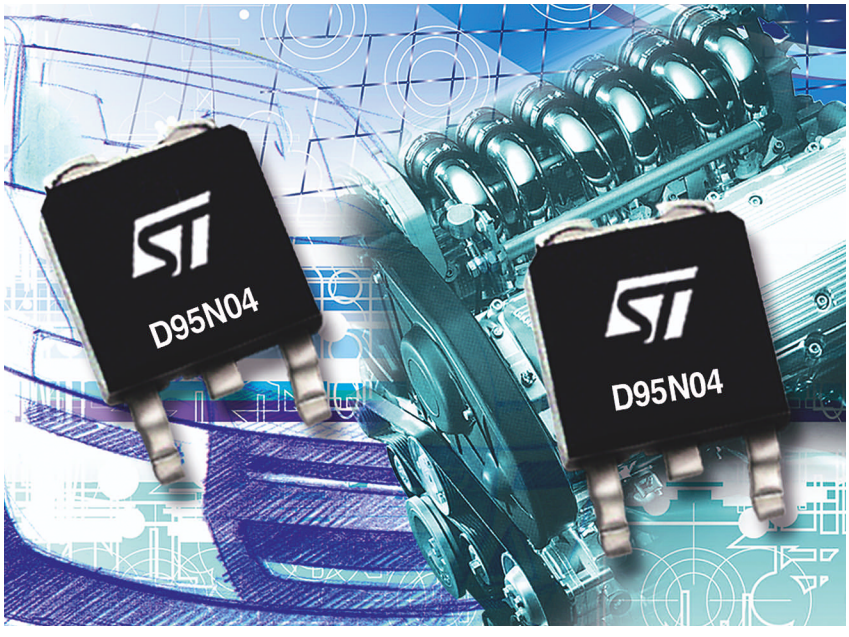

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STMicroelectronics, www.st.com

Chip set comprises control and synchronous MOSFETs

The IRF7823PbF and IRF7832-ZPbF chip set targets use as two-phase synchronous-buck-converter circuits requiring a control MOSFET and two synchronous MOSFETs per phase. By optimizing conduction, switching, and body-diode losses, the devices maximize efficiency and power density. The control IRF7823PbF FET has a 9.1-nC gate charge and a 3.2-nC gate-to-drain charge; the IRF7832ZPbF has a 4.5V on-resistance and suits synchronous FET functions. The IRF7823PbF and IRF7832ZPbF cost 50 and 88 cents (10,000), respectively.

International Rectifier, www.irf.com

Dual-bootstrapped MOSFET driver features output disable

The dual-bootstrapped, single-phase,12V NCP3418B MOSFET gate driver can drive gates of high- and low-side power MOSFETs in a synchronous buck converter. Capable of driving a 3000-pF load, the device has a 25-nsec propagation delay and a 20-nsec transition time. Features include cross-conduction-protection circuitry, a floating-top driver supporting 30V boost voltages, an input signal controlling the upper and lower gate outputs, and output-disable-control switching of both MOSFETs. The NCP3418B costs 59 cents (3000).

On Semiconductor, www.onsemi.com

Integrated MOSFET and drivers feature operation as high as 1 MHz

The SiC714CD10 and SiC711-CD10 high-speed, integrated MOSFET and drivers suit 3.3, 5, and 12V intermediate-bus-architecture environments. Simplifying the single-phase and multiphase dc-to-dc design, the converters integrate a control MOSFET, a synchronous MOSFET, and a driver circuit into a PowerPAK MLF package. Both devices target 12V-to-logic-level conversion and have a 100-kHz to 1-MHz switching-frequency range. The devices cost $2 (100,000).

Vishay, www.vishay.com

High-current drivers suit large MOSFETs and IGBTs

Providing a 12A peak output current, the TC445X MOSFET-driver circuits feature latch-up immunity and a 15-nF-in-27-nsec drive speed. This feature provides ruggedness and high-power switching speeds and sharp edges for driving large MOSFETs and IGBTs (insulated-gate bipolar transistors) in high-efficiency switch-mode power supplies. The high-current, high-speed TC445X comes in SOIC-8 and PDIP-8 packages and costs $1.44 (10,000).

Microchip Technologies, www.microchip.com

productroundup

DISCRETE SEMICONDUCTORS

MOSFET-driver relay has a high short-circuit current

These dual-photovoltaic MOSFET-driver SSRs (solid-state relays) provide a 14.6V open-circuit voltage. The VO1263AB suits MOSFET and SCR (silicon-controlled-rectifier) gate-drive applications and includes high-side switches, power solid-state relays, flowing power supplies, and isolation amplifiers. Features include a 14.6V open-circuit voltage, allowing use with a wide range of low-voltage MOSFETS, and a 42A short-circuit current—a 2.5-times improvement over the vendor's previous model. Available in a lead-free DIP-8 package, the VO1263AB costs $1.51 (10,000).

Vishay, www.vishay.com

COMPUTERS & PERIPHERALS

2.5-in.-hard-drive family increases capacity to 120 Gbytes

The 2.5-in. M60 SATA series and the M60 series, new additions to the SpinPoint hard-drive family, include 8 Mbytes of onboard cache and a high-performance, 5400-rpm spindle speed. The M60 SATA series includes the 100-Gbyte HM100JI and the 120-Gbyte HM120JI for $170 and $200, respectively, and the M60 series features the 100-Gbyte HM100JC and the 120-Gbyte HM120JC for $150 and $180, respectively.

Samsung Electronics, www.samsung.com

Storage processor features five high-speed SATA-II ports

With five high-speed, 3-Gbps SATA-II ports, the SiI 4726 SteelVine storage processor supports auto rebuild, auto failover, hot swap, and hot spare. At 100 Gbytes/hour, the device re-establishes a mirrored-drive set after replacing a failed drive. Features include 2.5 Tbytes of storage; 230 Mbyte/sec I/O throughput; and support for RAID 0, RAID 1, RAID 10, concatenation, and JBOD-port-multiplier configurations. The processor enables multiple RAID partitions on single hard drives. Compatible with SATA-compliant host ports without the need for a driver, BIOS extension, or host software, the SiI 4726 costs $27 (5000).

Silicon Image, www.siliconimage.com

SATA hard drives have 500-Gbyte capacity

The SATA WD Caviar SE16 desktop-class hard drives feature a 500-Gbyte capacity. Delivering a 7200-rpm performance, they also feature a 300-Mbps transfer rate, 16-Mbyte cache, and native-command queuing. The WD5000KS drives cost $349.99.

Western Digital, www.westerndigital.com

PCI Express broadcast decoder supports all audio/video standards

With 1.0a PCI Express compliance and a 1.1-ready audio/video-broadcast decoder, the CX23885 PCI Express broadcast decoder targets television and radio applications on the PC. Capturing analog- and digital-television broadcasts, the device supports worldwide audio/video standards and integrates all required functions for per-

COMPUTERS & PERIPHERALS

forming television and external audio/video capture. Available in a 14×14-mm ETQFP-128 package, the CX23885 costs $10.

Conexant Systems, www.conexant.com

EMBEDDED SYSTEMS

Carrier blade hosts as many as four AdvancedMC modules

Targeting IBM BladeCenter systems, the SBS BCT4-AMC1 AdvancedMC carrier blade can host as many as four AdvancedMC modules. These modules create application-specific blades from standard, off-the-shelf SBS Telum modules and other third-party AdvancedMC cards. The blade provides two AdvancedMC bays accessible from the front and two internal bays on either side. Support for hot-swap capabilities for the front-bay modules and the carrier blade reduces equipment downtime. The BCT4-AMC1 BladeCenter carrier blade costs $1950.

SBS Technologies, www.sbs.com

CompactPCI 2.16 computation blade features AMD-processor options

Based on 64-bit, single- and dual-core AMD Opteron processors, the CPC5564 CompactPCI 2.16 computation blade targets high-end telecommunications, defense and homeland security, and commercial applications. Processor options include 64-bit AMD Opterons in either a 2.2-GHz single core or a 1.8-GHz dual core. Key features include a 2-, 4-, or 8-Gbyte memory option; PICMG 2.16 and PICMG 2.9 IPMI compatibility; an onboard-managed Ethernet switch; and a dual-gigabyte interface. The single-board computer also provides a 64-bit, eight-lane PCI-X PMC/PCI Express XMC slot, USB 2 support, and four-channel SATA or one-

EMBEDDED SYSTEMS

channel PATA. An optional onboard hard drive is also available. The CPC-5564 costs $2995.

Performance Technologies, www.pt.com

Wireless family adds three development kits

The Xbee-Pro starter kit and Xbee starter kit target point-to-point wireless-communications applications. Establishing a reliable RF link in minutes, the devices include two Xbee-Pro or two Xbee modules with integrated wire-whip antennas, as well as an RS-232- and USB-development board. Maximizing the mesh-network capabilities of the ZigBee standards, the Xbee Professional developer's kit features five OEM RF modules and five enhanced-development boards with S-232 or USB connectivity. The XBee-Pro starter kit, XBee starter kit, and XBee Professional developer's kit cost $179, $129, and $339, respectively.

Maxstream Inc, www.maxstream.net

PCI CPU implements a flexible design

The flexibility of the Pentium M-processor-based Eurocom 300 PCI CPU allows its use in multiple applications. A basic version allows you to use it as a computer core without requiring the I/O connections of typical PCs. The device has two Ethernet interfaces and an optional, 1-Gbps Ethernet controller separating the machine network and the control system and supporting real-time Ethernet connections. A second version offers PC-typical interfaces on the front panel. For special applications, users can access two serial interfaces. The device suits closed- and open-loop control tasks through the use of a configurable timer and a nonvolatile, 512-kbyte memory area, which functions in SRAM in operation, EEPROM in de-energized mode, and automatic programming on power-down mode. Available OSs include Windows XP, Windows embedded XP, Linux, and Elinos. The Eurocom 300 costs $950.

American Eltec, www.americaneltec.com

Software-radio-transceiver module adds digital-downconverter core

Using a core implemented in a Xilinx FPGA, the 7140-430 software-radio transceiver provides 256 individually tunable receiver channels in a PMC/XMC-transceiver module. The module's front end accepts two analog HF inputs and transformer-couples the inputs into 14-bit ADCs at 105 MHz. Digitized-output signals pass to a Virtex-II Pro XC2VP50 FPGA, implementing the downconverter core. A channelizer stage generates 1024 fixed, adjacent, overlapping frequency channels with 75-dB, alias-free performance. A 256-output-switch matrix follows the channelizer, providing the coarse-tuning function. The 7140-430 software-radio transceiver costs $14,995.

Pentek Inc, www.pentek.com

Stamp-sized single-chip computer uses flash memory

Based on Analog Devices' Adu-C7020 MicroConverter chip with an ARM7 core, the ForthStamp single-chip-computer OS is available in flash memory to drive all peripheral devices. Measuring 1.25×0.75 in., the ForthStamp costs $35, including all software-development tools. A UART33 companion kit, allowing the device to communicate with PCs through a communications port, is available for $20.

Offete Enterprises, www.offete.com

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realitycheck

YESTERDAY'S HYPE MEETS TODAY'S REALITY

STATS Originally targeted Quake II game engine / To-date development time: approximately nine years

Long-promised game may yet appear

The *Duke Nukem* series, which its developer, 3D Realms, unveiled in July 1991, was one of the pioneering success stories in PC games. By April 1997, when 3D Realms pre-announced *Duke Nukem Forever*, the family comprised *Duke Nukem I*, *II*, and *3D*. The fourth title suffered a series of miscues and restarts, leading to the gaming community's frequently citing it as a notable example of "vaporware." Pundits said that the title's initials alternatively meant Did Not Finish and referred to the product as *Duke Nukem Whenever*, *Duke Nukem Whatever*, *Duke Nukem If Ever*, *Duke Nukem Taking Forever*, and *Duke Nukem Never*.

Surprisingly, however, the project may yet see the light of day. According to company co-founder George Broussard, *Duke Nukem Forever* is in "full production." In production, however, doesn't apparently mean finished, as it does with a hardware product, because, Broussard also says, "There's a lot that's finished. All the guns are finished. Most of the creatures are finished. We're just basically pulling it all together and trying to make it fun."

Will you ever be able to play *Duke Nukem Forever*, and, if so, will the final product be worth the wait? Only time will tell; tune in to Slashdot to see what that unforgiving tech community thinks (http://games.slashdot.org/article.pl?sid=06/02/02/0124200).—by Brian Dipert

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Chipcon mouser.com/chipcon/a

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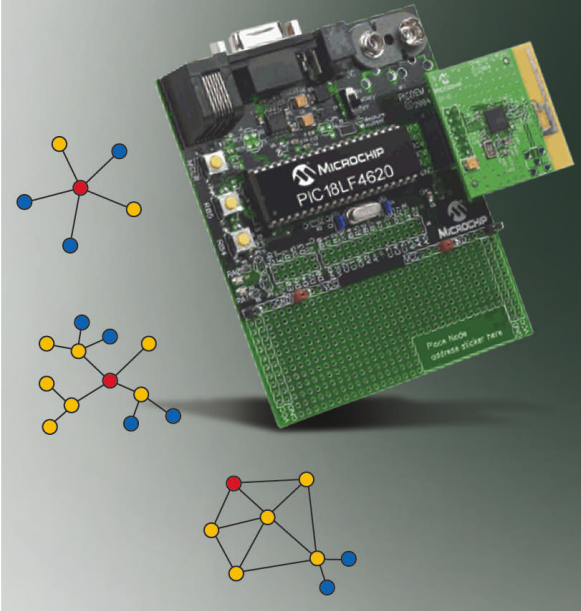

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SILICON LABORATORIES mouser.com/silabs/a

Microchip PICDEM™ Z Demonstration Kit

This kit is an easy-to-use ZigBee™ Technology wireless communication protocol development and demonstration platform. The kit includes the ZigBee protocol stack and two PICDEM Z boards, each with an RF daughter card. The demonstration board is also equipped with a 6-pin modular connector to interface directly with Microchip's MPLAB® ICD 2 in-circuit debugger (DV164005).

MICROCHIP ouser.com/microchip/a

Freescale ZigBee™ Evaluation Kits

The kit is a short range, low power, 2.4 GHz ISM band transceiver which contains a complete 802.15.4 PHY/MAC, the ZigBee protocol stack supporting star, and mesh networking. The MC13193 can be a stand-alone transceiver or part of the Freescale ZigBee-ready platform when combined with an appropriate microcontroller.

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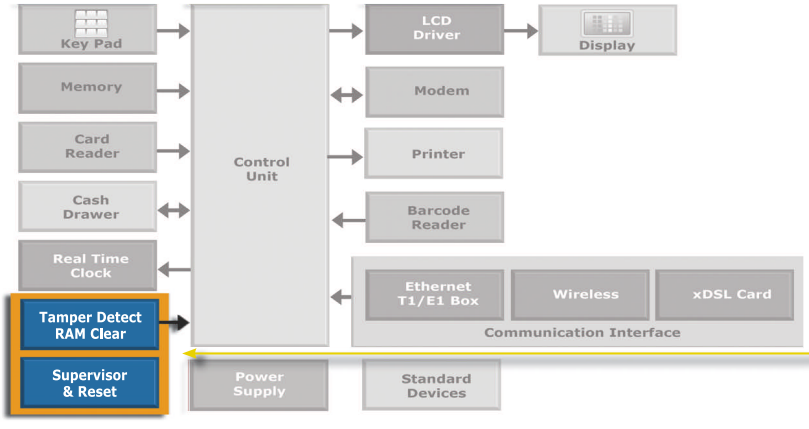

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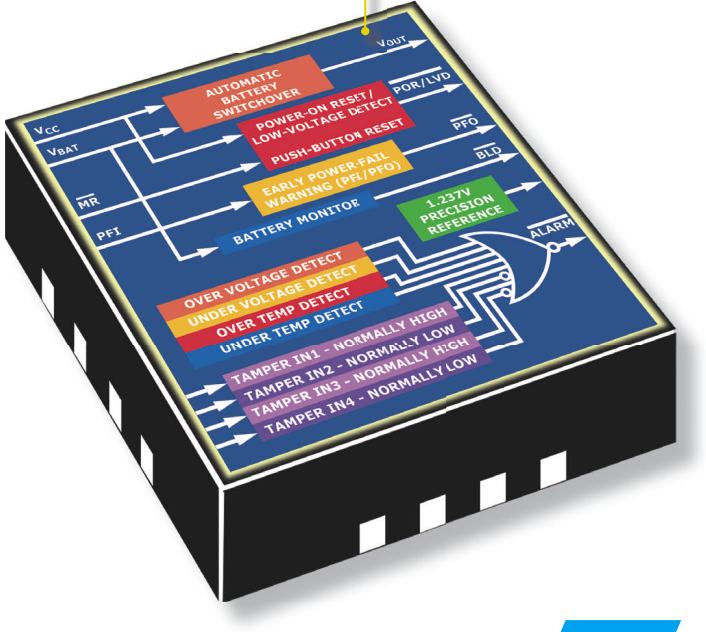

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